5.0V/150mA Low-Drop Fixed-Voltage Regulator

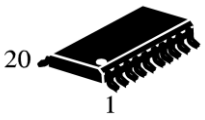
IK4993

GENERAL DESCRIPTION

The IK4993 is a monolithic integrated low-drop fixed voltage regulator 150mA with low current consumption.

The regulating output voltage element consists in a p-channel MOS and the regulation is performed regardless of input voltage transients up to 40V. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. The IK4993 is protected against short circuit and an over-temperature protection switches off the IC in case of extremely high power dissipation.

Reset and watchdog make this device particularly suitable to supply microprocessor systems in automotive applications.



Ordering Information

IK4993D	SOP-16
IK4993HD	SOP-20

FEATURES

- Operating DC supply voltage range 5.6V to 31V
- Output voltage tolerance: ≤ ±2%
- Low-drop voltage ≤ 400mV
- Current capability up to 150mA
- Reset circuit sensing the output voltage down to 1V
- Programmable reset pulse delay with external capacitor
- Watchdog
- Programmable watchdog timer with external capacitor
- Enable input for enabling/disabling the watchdog functionality
- Thermal shutdown and short circuit protection
- T_j operation temperature -40 to +150°C
- Certified by AEC-Q100 standard

BLOCK DIAGRAM.

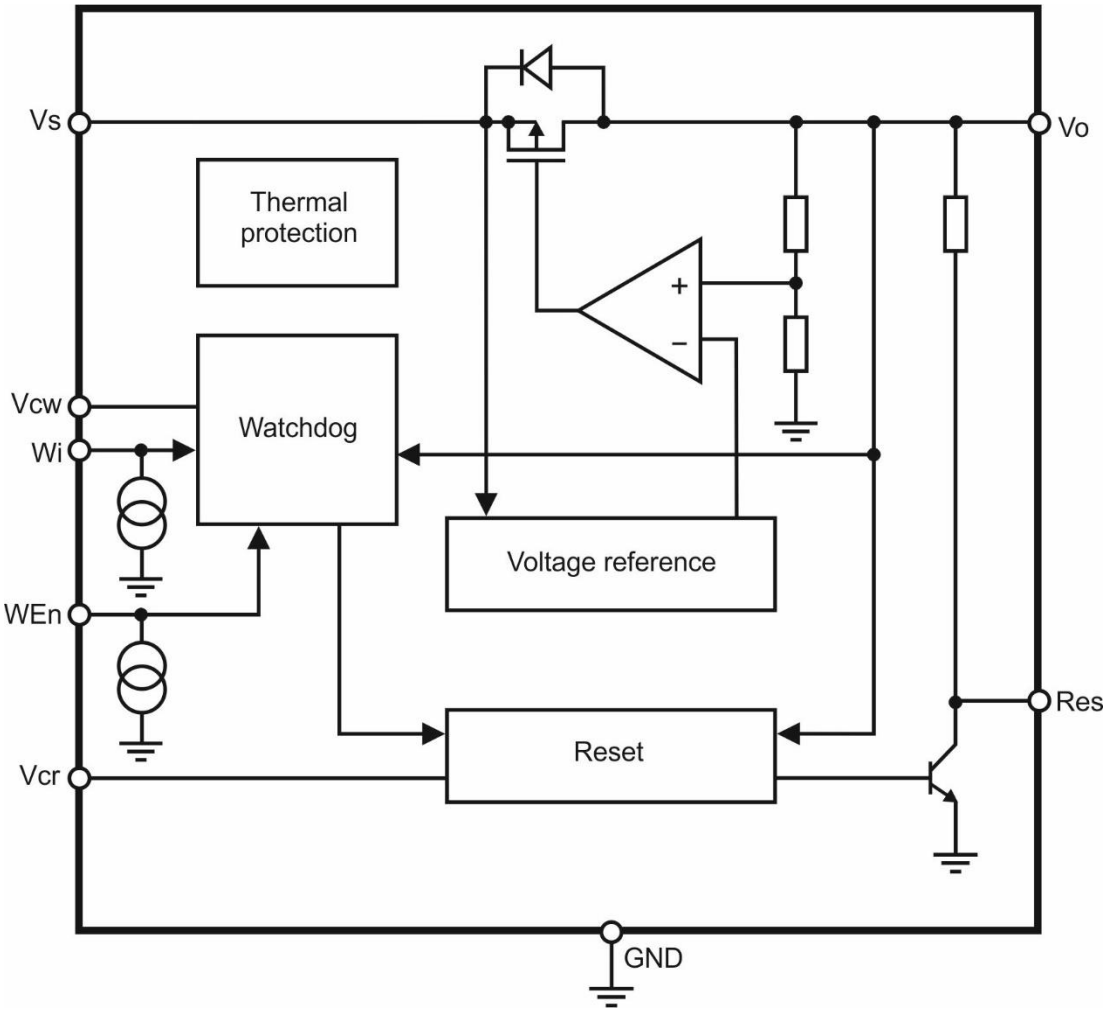


Fig. 1. Block diagram.

Table 1. PIN LIST AND DESCRIPTIONS.

Name	Pin (8 pin package)	Pin (20 pin package)	Description
WEn	1	1	Watchdog Enable input. If high watchdog functionality is active.
GND	2	4	Ground reference.
GND	-	5, 6, 15, 16	Ground. Connected these pins to a heat spreader ground.
Res	3	7	Reset output. It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low. Leave floating if not used.
V_{CR}	4	10	Reset timing adjust. A capacitor between V_{CR} pin and GND, sets the reset delay time (trd).
V_{CW}	5	11	Watchdog timer adjust. A capacitor between V_{CW} pin and GND, sets the time response of the watchdog monitor.
W_I	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated. Connect to ground if not used.
V_O	7	17	Voltage regulator output. Block to ground with a capacitor >100nF (needed for regulator stability).
V_S	8	20	Supply voltage. Block to ground directly at IC pin with a capacitor.
N.C.	-	2, 3, 8, 9, 12, 13, 18, 19	Not connected.

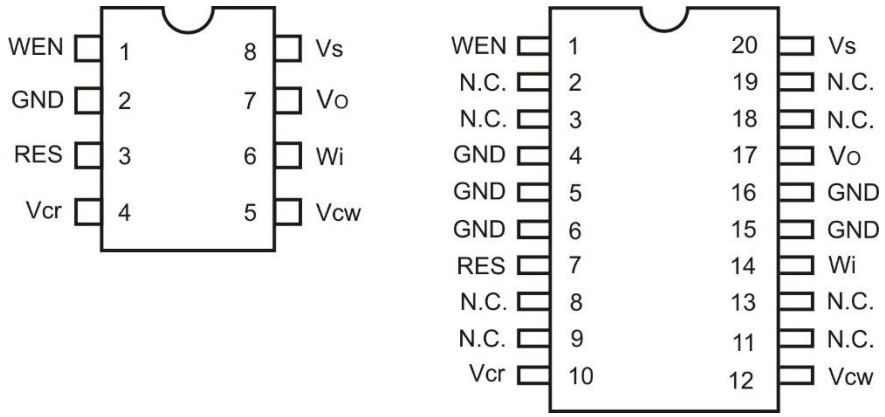


Fig. 2. Pins configuration.

Table 2. ABSOLUTE MAXIMUM RATINGS.

Tj = – 40 to 150 °C

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 40	V
I_{VS}	Input current	Internally limited	
V_O	DC output voltage	-0.3 to 6	V
I_O	DC output current	Internally limited	
V_{WI}	Watchdog input voltage	-0.3 to V_O + 0.3	V
V_{OD}	Open drain output voltage	-0.3 to V_O + 0.3	V
I_{OD}	Open drain output current	Internally limited	
V_{CR}	Reset delay voltage	-0.3 to V_O + 0.3	V
V_{CW}	Watchdog delay voltage	-0.3 to V_O + 0.3	V
V_{WEn}	Watchdog Enable input voltage	-0.3 to V_O + 0.3	V
Tj	Junction temperature	-40 to 150	˚C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV
V_{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. THERMAL DATA.

Symbol	Parameter	Value	Unit
Rth-jamb	Thermal resistance Junction to Ambient: 8 pins package 20 pins package	 130 51	 ˚C/W ˚C/W

Note:

The values quoted are for PCB FR4 area = 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm , copper areas: SO-8= 2 cm2, SO-20= 6 cm2.

Electrical Characteristics.

Values specified in this section are for Vs =5.6V to 31V, Tj= - 40°C to +150°C unless otherwise stated.

Table 4. General parameters.

Pin	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vo	V_O	Output voltage	Vs = 6 to 31V Io = 1 to 150mA	4.9	5.0	5.1	V
Vo	Ishort	Short circuit current	Vs = 13.5V(1)	150	280	400	mA
Vo	Ilim (2)	Output current limitation	Vs = 13.5V(1)	150	320	500	mA
Vs, Vo	Vline	Line regulation voltage	Vs = 6 to 31V Io = 1 or 150mA			25	mV
Vo	Vload	Load regulation voltage	Io = 1 to 150mA Vs = 13.5V			25	mV
Vs, Vo	Vdp (3)	Drop voltage	Io = 150mA		200	400	mV
Vs, Vo	SVR	Ripple rejection	fr = 100 Hz (4)	55			dB
Vs, Vo	I_{qn_150}	Quiescent current	Vs=13.5V, Io=150mA, WEn = high		1.25	2	mA
Vs, Vo	I_{qn_50}	Quiescent current	Vs=13.5V, Io=50mA, WEn = high		470	1000	μA
Vs, Vo	I_{qn_1}	Quiescent current	Vs=13.5V, Io = 1mA, WEn = high		100	180	μA
Vs, Vo	Iqs	Quiescent current with watchdog regulator disabled	Vs=13.5V, Io = 1mA, WEn = low		79	125	μA
	T_{jp}	Thermal protection temperature		150		190	˚C
	T_{jph}	Thermal protection temperature hysteresis			10		˚C

Note:

1. See Fig. 6.

2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at Vs=13.5V and Io= 75mA.

3. Vs-Vo measured when the output voltage has dropped 100mV from its nominal value obtained at Vs=13.5V and Io= 75mA.

4. Guaranteed by design.

Table 5. Reset output parameters.

Pin	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Res	V_{Res_l}	Reset output low voltage	Rext = 5kΩ to Vo, Vo > 1V			0.4	V
Res	I_{Res_h}	Reset output high leakage current	V_{Res} = 5V			1	μA
Res	R_p_u	Pull up internal resistance	With respect to Vo	12	25	50	kΩ
Res	Vo_th	Vo out of regulation threshold	Vs = 6 to 31V, Io = 1 to 150mA	6%	8%	10%	Below Vo_ref
V_{CR}	Vrlth	Reset delay circuit low threshold	Vs = 13.5V	10%	13%	16%	Vo_ref
V_{CR}	Vrhth	Reset delay circuit high threshold	Vs = 13.5V	44%	47%	50%	Vo_ref
V_{CR}	I_{CR}	Charge current	Vs = 13.5V	8	17.6	30	μA
V_{CR}	I_{DR}	Discharge current	Vs = 13.5V	8	17.6	30	μA
Res	Trr_2	Reset reaction time (1)	Vo = Vo_th - 100mV	100	275	1000	μs
Res	Trd	Reset delay time	Vs = 13.5V, Ctr = 1nF	65		150	ms

Note:
When Vo becomes lower than 4V, the reset reaction time decreases down to 2μs assuring a faster reset condition in this particular case.

Table 6. Watchdog parameters.

Pin	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Wi	Vih	Input high voltage	Vs = 13.5V	3.5			V
Wi	Vil	Input low voltage	Vs = 13.5V			1.5	V
Wi	Vih_hyst	Input hysteresis	Vs = 13.5V		500		mV
Wi	Ii	Pull down current	Vs = 13.5V		10	20	μA
Vcw	Vwhth	High threshold	Vs = 13.5V	44%	47%	50%	Vo_ref
Vcw	Vwlth	Low threshold	Vs = 13.5V	10%	13%	16%	Vo_ref
Vcw	Icwc	Charge current	Vs = 13.5V, Vcw = 0.1V	4	8	14	μA
Vcw	Icwd	Discharge current	Vs = 13.5V, Vcw = 2.5V	1.0	2.13	4.5	μA
Vcw	Twop	Watchdog period	Vs = 13.5V, Ctw = 47nF	25	50	90	ms
Res	twol	Watchdog output low time	Vs = 13.5V, Ctw = 47nF	6	10.5	22	ms

Table 7. Watchdog Enable parameters.

Pin	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
WEn	W_{En_low}	Enable input low voltage				1	V
WEn	W_{En_high}	Enable input high voltage		3			V
WEn	W_{En_hyst}	Enable input hysteresis		500	800	1100	mv
WEn	Ileak	Pull down current	WEn = 5V	2	8	20	μA

Test circuits.

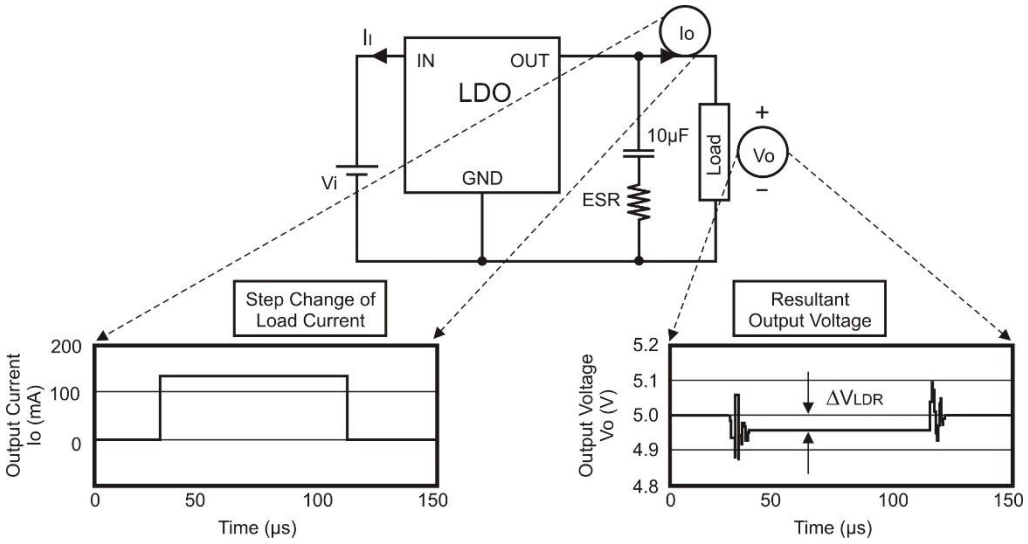


Fig. 3. Load regulation test circuit.

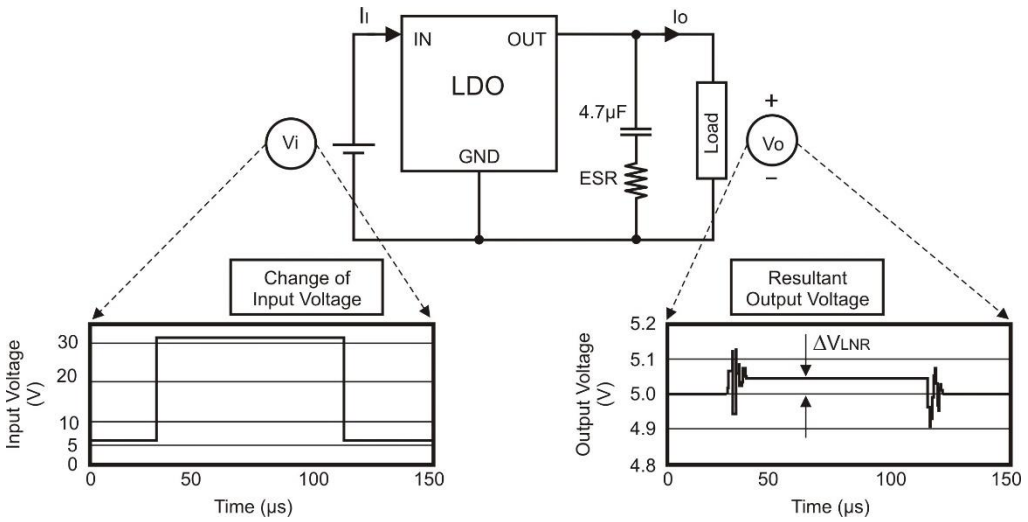


Fig. 4. Line regulation test circuit.

Application information.

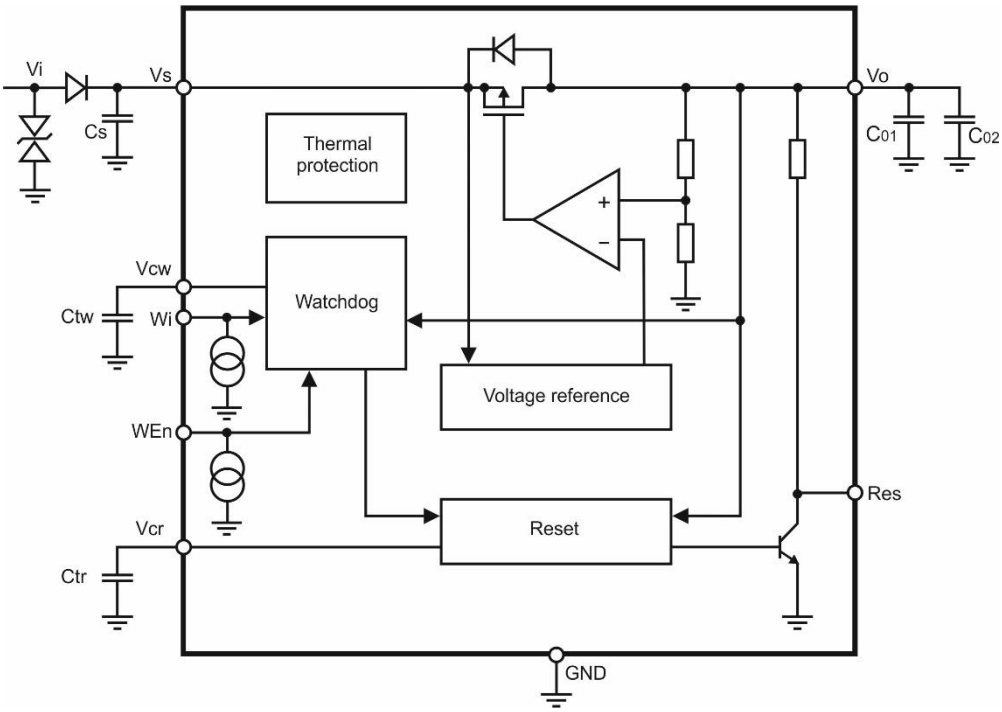


Fig. 5. Application circuit.

Voltage regulator.

Voltage regulator uses a p-channel transistor as a regulating element. With this structure, very low dropout voltage at current up to 500mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated.

A short circuit protection to GND is provided.

The voltage regulator watchdog functionality can be disabled by putting WEn low.

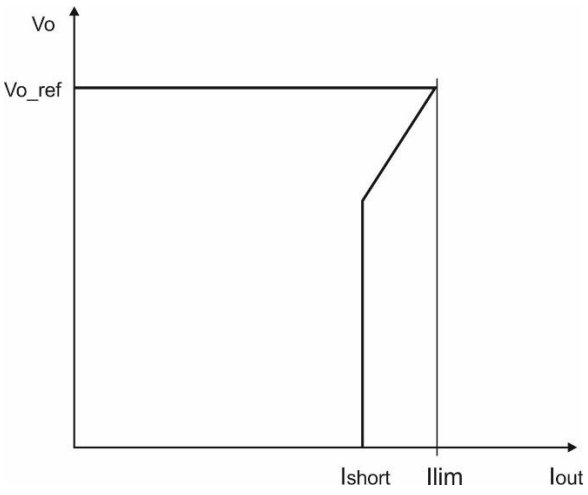


Fig. 6. Behavior of current limitation.

Reset.

The reset circuit supervises the output voltage Vo. The Vo_th reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than Vo_th then Res goes low with a reaction time trr. The reset low signal is guaranteed for an output voltage Vo greater than 1V. When the output voltage becomes higher than Vo_th then Res goes high with a delay trd. This delay is obtained by an internal oscillator.
The oscillator period is given by:

Tosc = [(Vrhth-Vrlth) x Ctr] / Icr + [(Vrhth-Vrlth) x Ctr] / Idr

where:
I_{CR}: is an internally generated charge current
I_{DR}: is an internally generated discharge current
Vrhth, Vrlth: two voltages defined with the output voltage and a resistor output divider.
Ctr: is an external capacitance.
trd is given by:

trd = 512 x Tosc

Reset is active when En is high.

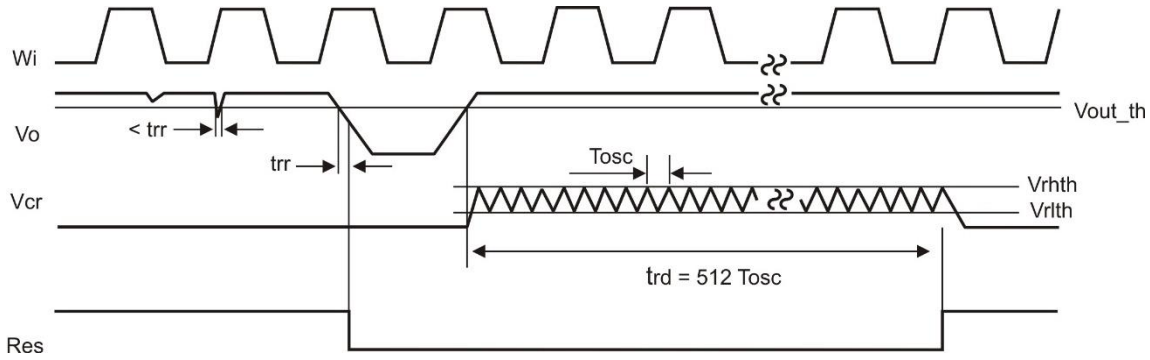


Fig. 7. Reset timing diagram.

Watchdog.

A connected microcontroller is monitored by the watchdog input Wi. If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, Ctw. The watchdog circuit discharges the capacitor Ctw, with the constant current Icwd. If the lower threshold Vwlth is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold Vwlth. In order to calculate the minimum time t, during which the micro-controller must output the positive edge, the following equation can be used:

(Vwhth-Vwlth) x Ctw = Icwd x t

Every Wi positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, Vwhth, the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor Ctw.

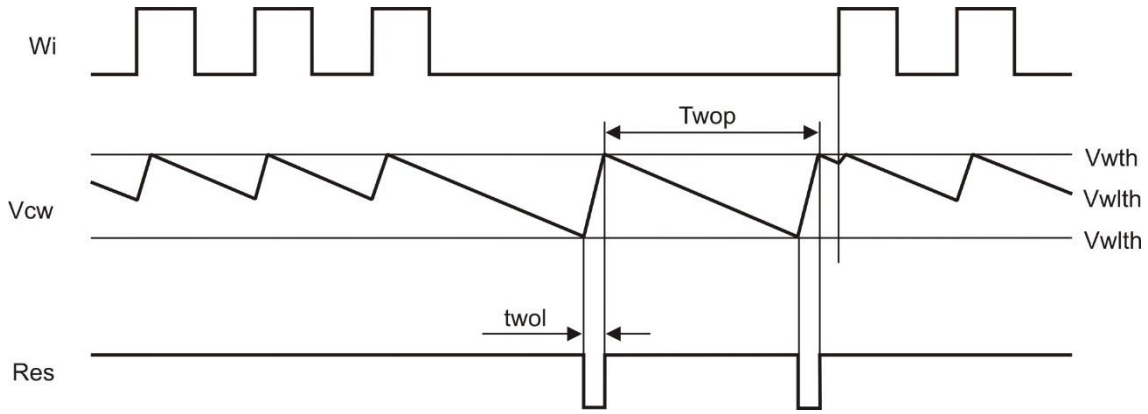


Fig. 8. The timing diagram of the watchdog.

Power Dissipation and Junction Temperature.

Most LDO regulators specify a junction temperature to assure their operations; the maximum junction temperature allowable without damaging the device is also specified. This restriction limits the power dissipation that the regulator can handle in any given application. To ensure that the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, PD (max), and the actual dissipation, PD, which must be less than or equal to PD (max).

The maximum power dissipation limit is determined using the following equation:

$$PD\ (max) = T_{Jmax} - T_A / R_{JA}$$

Where

T_{Jmax} is the maximum allowable junction temperature.

R_{JA} is the thermal resistance junction-to-ambient for the package.

T_A is the ambient temperature.

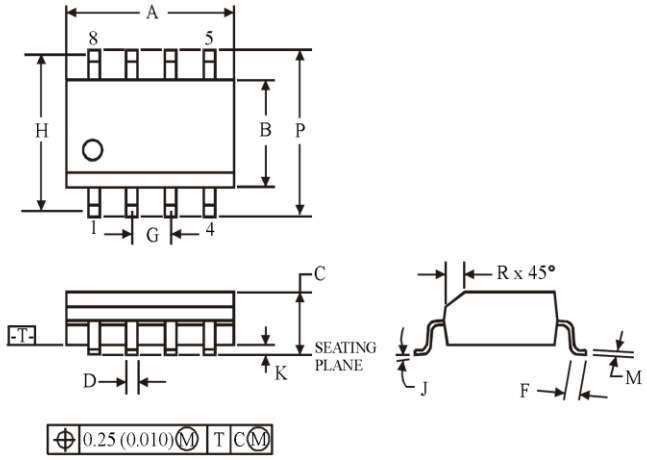
The regulator power dissipation is calculated using:

$PD = (V_{IN} - V_{OUT}) \times I_{OUT}$

Package information.

D SUFFIX SOP

(MS - 012AA)



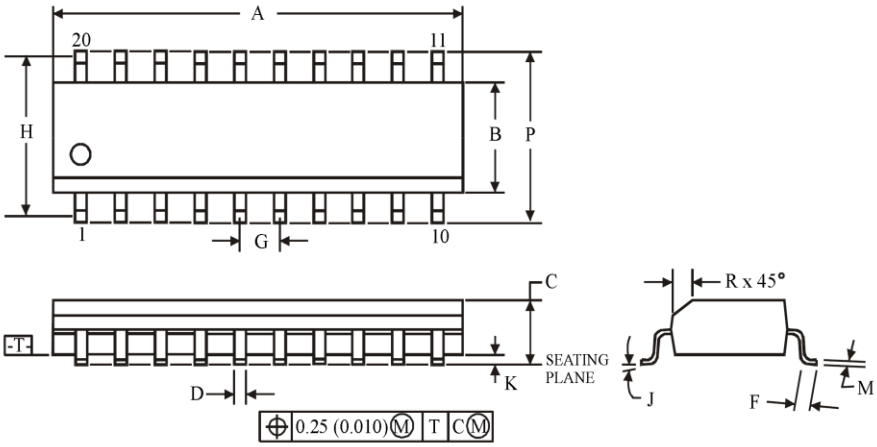
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B – 0.25 mm (0.010) per side.

D SUFFIX SOIC

(MS - 013AC)



	Dimension, mm	
Symbol	**MIN**	**MAX**
A	12.60	13.00
B	7.40	7.60
C	2.35	2.65
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.10	0.30
M	0.23	0.32
P	10.00	10.65
R	0.25	0.75

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B – 0.25 mm (0.010) per side.