

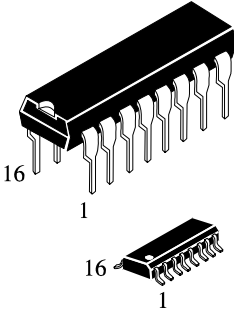
IN74HC4015A

Dual 4-Bit Shift Register
High-Performance Silicon-Gate CMOS

The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device consists of two identical independent 4-stage serial-input/parallel-output registers. Each register has independent Clock and Reset inputs as well as a single serial Data input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the Data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line.

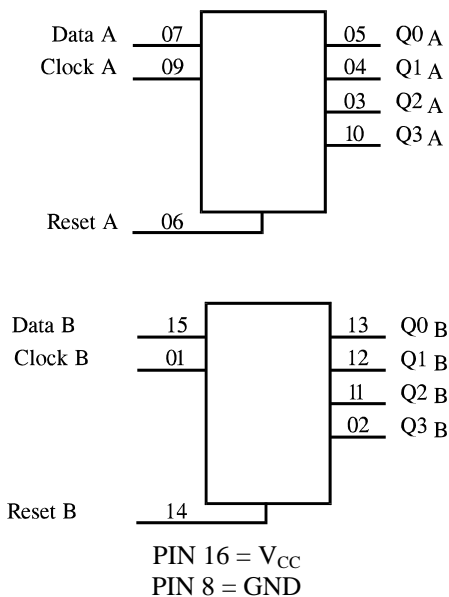
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices



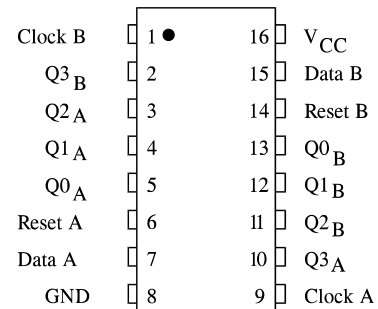
N SUFFIX PLASTIC
 D SUFFIX SOIC

ORDERING INFORMATION
 IN74HC4015AN Plastic
 IN74HC4015AD SOIC
 $T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
Clock	Data	Reset	Q_0	Q_n
	L	L	L	Q_{n-1}
	H	L	H	Q_{n-1}
	X	L	Q_0^*	Q_n^*
X	X	H	L	L

* = No Change
 X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			
	V _{CC} =2.0 V	0	1000	ns
	V _{CC} =4.5 V	0	500	
	V _{CC} =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	8.0	80	160	μA

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figure 2)	2.0	6	4.8	4	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 2 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 1 and 5)	2.0	205	255	310	ns
		4.5	41	51	62	
		6.0	35	43	53	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Latch)	Typical @25°C, $V_{CC}=5.0\text{ V}$			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	140			

TIMING REQUIREMENTS($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, D to Clock (Figure 4)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
t_h	Minimum Hold Time, Clock to D (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_{rec}	Minimum Recovery Time, Reset to Clock (Figure 1)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_w	Minimum Pulse Width, Reset (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Clock (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

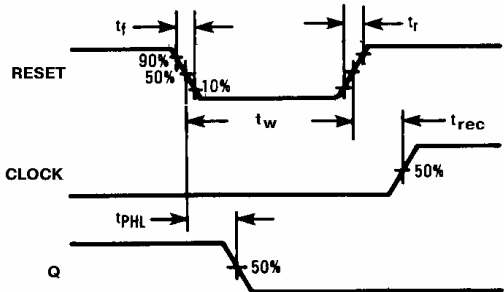


Figure 1. Switching Waveforms

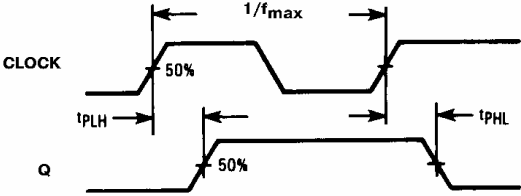


Figure 2. Switching Waveforms

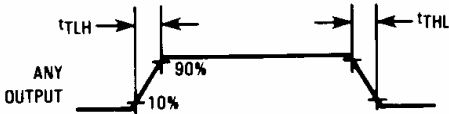


Figure 3. Switching Waveforms

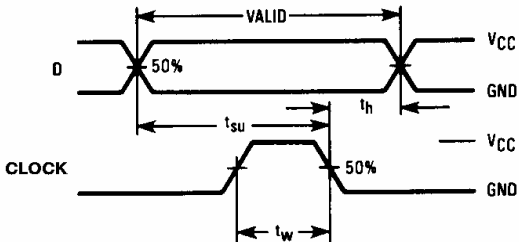
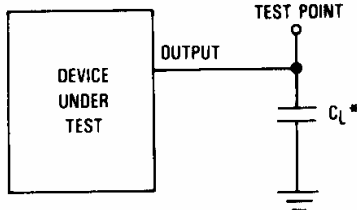


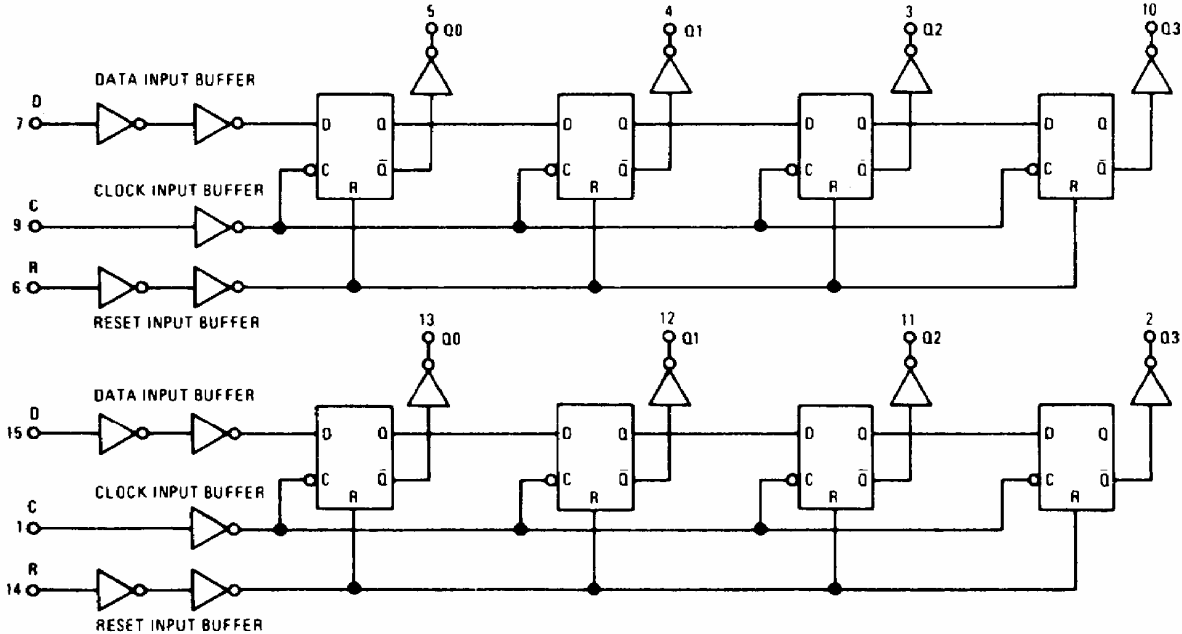
Figure 4. Switching Waveforms



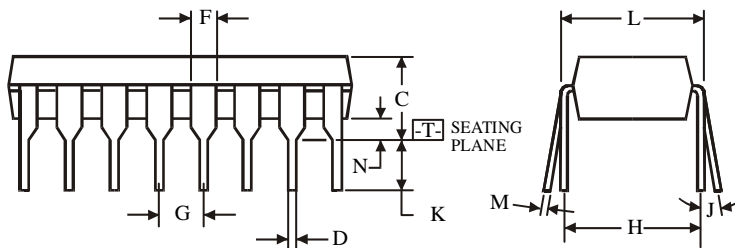
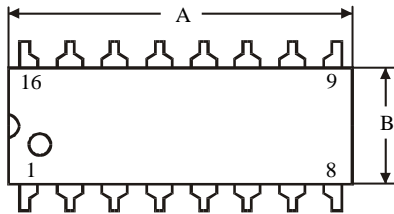
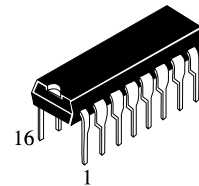
*includes all probe and jig capacitance.

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM



**N SUFFIX PLASTIC DIP
(MS - 001BB)**



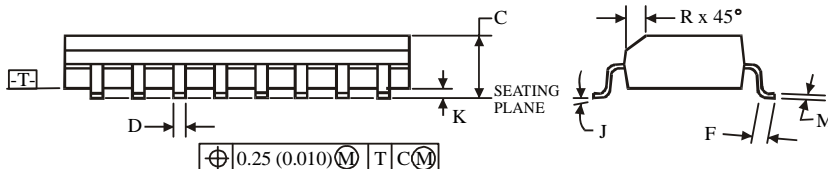
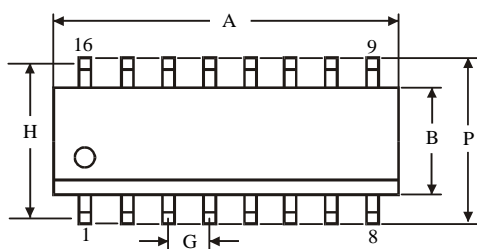
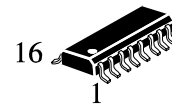
$\oplus 0.25 (0.010) \text{ (M) T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**D SUFFIX SOIC
(MS - 012AC)**



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	9.8	10
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5