

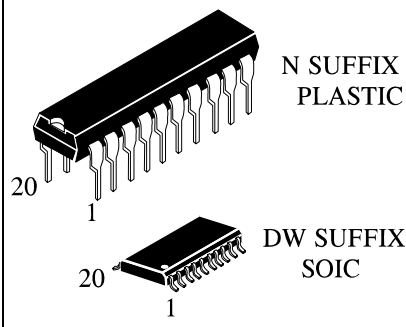
**IN74HCT245A**

**Octal 3-State Noninverting  
Bus Transceiver  
High-Performance Silicon-Gate CMOS**

The IN74HCT245A is identical in pinout to the LS/ALS245. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

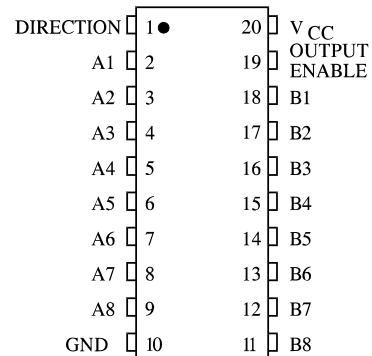
The IN74HCT245A is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A

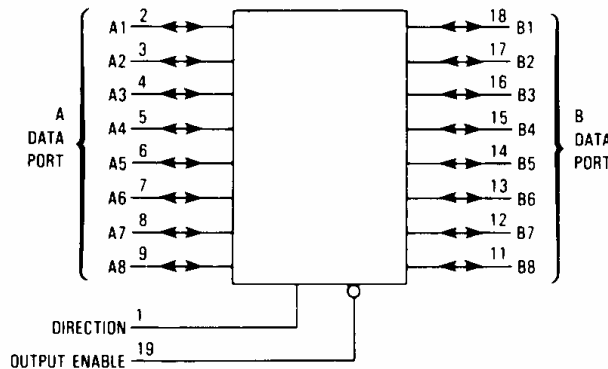


**ORDERING INFORMATION**  
 IN74HCT245AN Plastic  
 IN74HCT245ADW SOIC  
 IN74HCT245ATDS SOIC  
 $T_A = -55^\circ$  to  $125^\circ$  C for all packages

**PIN ASSIGNMENT**



**LOGIC DIAGRAM**



PIN 20 =  $V_{CC}$   
 PIN 10 = GND

**FUNCTION TABLE**

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High Impedance State)

X = don't care

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: : - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND, Pin 1 or 19	5.5	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND, I/O Pins	5.5	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	5.5	4.0	40	160	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>IN</sub> =2.4 V, Any One Input V <sub>IN</sub> =V <sub>CC</sub> or GND, Other Inputs I <sub>OUT</sub> =0μA	5.5	≥-55°C	25°C to 125°C		mA
				2.9	2.4		

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, A to B or B to A (Figures 1 and 3)	22	28	33	ns
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	32	40	48	ns
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
$C_{IN}$	Maximum Input Capacitance (Pin 1 or Pin 19)	10	10	10	pF
$C_{OUT}$	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	15	15	15	pF

$C_{PD}$	Power Dissipation Capacitance (Per Enable Output)	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$			pF
	Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	97			

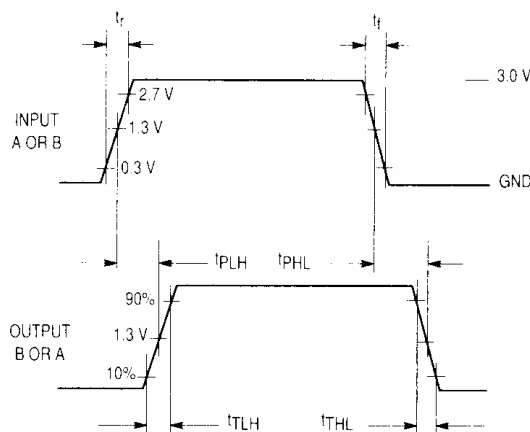


Figure 1. Switching Waveforms

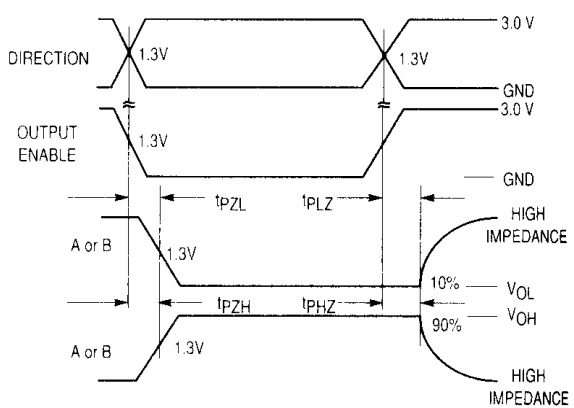
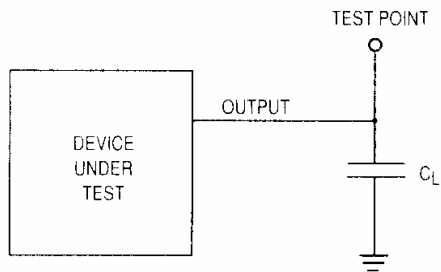
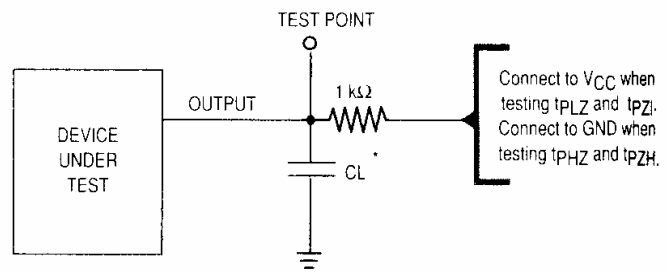


Figure 2. Switching Waveforms



\* Includes all probe and jig capacitance

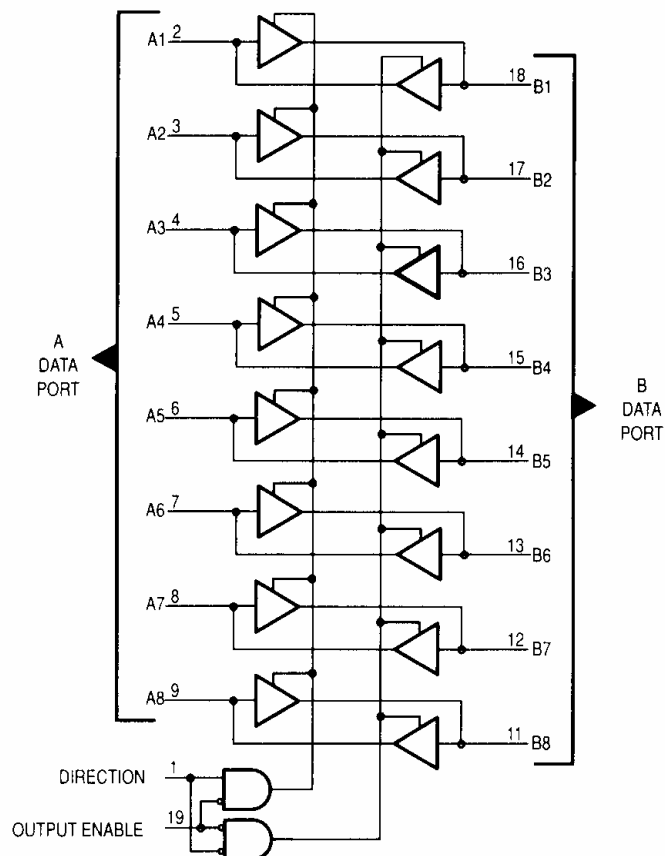
**Figure 3. Test Circuit**



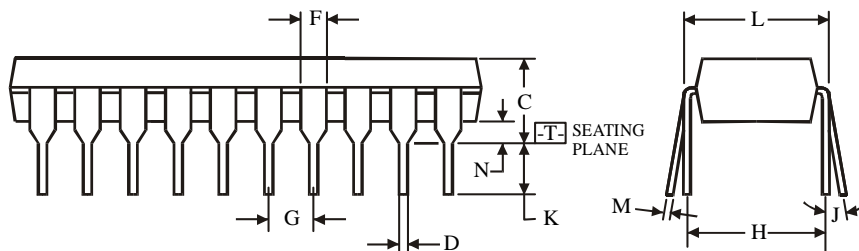
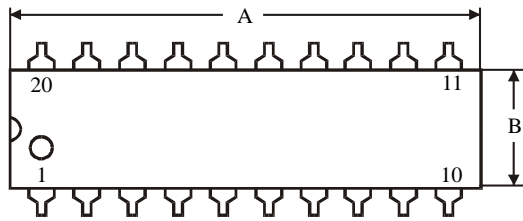
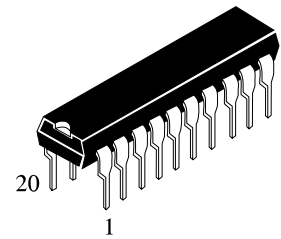
\* Includes all probe and jig capacitance

**Figure 4. Test Circuit**

**EXPANDED LOGIC DIAGRAM**



**N SUFFIX PLASTIC DIP  
(MS - 001AD)**



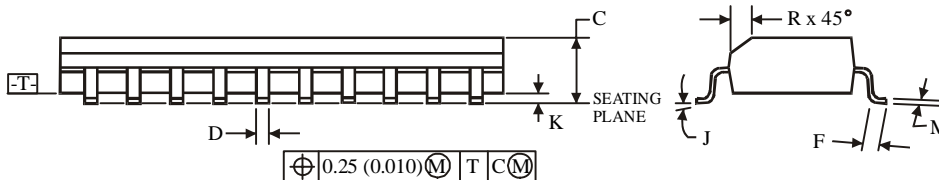
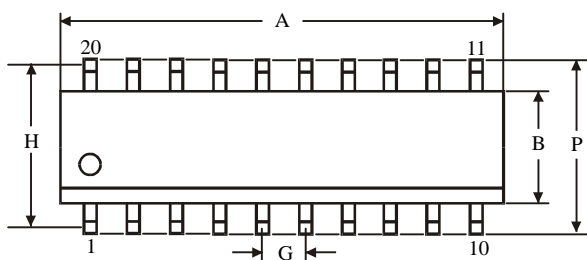
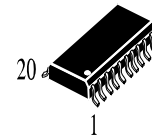
$\oplus 0.25 (0.010) \text{M} \text{T}$

**NOTES:**

- Dimensions "A", "B" do not include mold flash or protrusions.  
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	24.89	26.92
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**D SUFFIX SOIC  
(MS - 013AC)**



$\oplus 0.25 (0.010) \text{M} \text{T} \text{CM}$

**NOTES:**

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	12.6	13
B	7.4	7.6
C	2.35	2.65
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.1	0.3
M	0.23	0.32
P	10	10.65
R	0.25	0.75

TSSOP-20

