

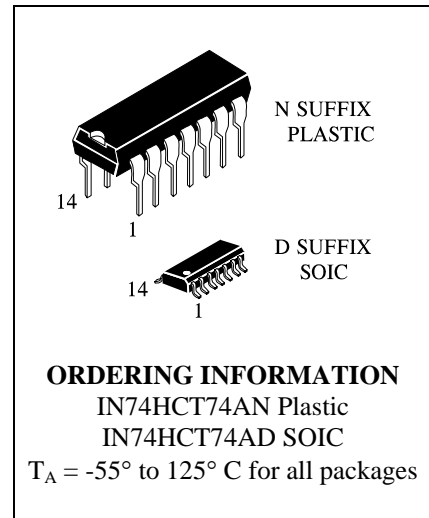
**IN74HCT74A**

**Dual D Flip-Flop with Set and Reset  
High-Performance Silicon-Gate CMOS**

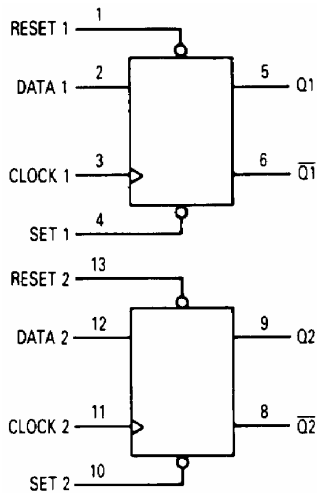
The IN74HCT74A is identical in pinout to the LS/ALS74. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and Q outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A



**LOGIC DIAGRAM**



PIN 14 =  $V_{CC}$   
PIN 7 = GND

**PIN ASSIGNMENT**

RESET 1	1 ●	14	$V_{CC}$
DATA 1	2	13	RESET 2
CLOCK 1	3	12	DATA 2
SET 1	4	11	CLOCK 2
Q1	5	10	SET 2
$\overline{Q1}$	6	9	Q2
GND	7	8	$\overline{Q2}$

**FUNCTION TABLE**

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H		H	H	L
H	H		L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H		X	No Change	

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.  
X = don't care

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA	5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA	5.5	0.1	0.1	0.1	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	5.5	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	5.5	1.0	10	40	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>IN</sub> =2.4 V, Any One Input V <sub>IN</sub> =V <sub>CC</sub> or GND, Other Inputs I <sub>OUT</sub> =0μA		≥-55°C	25°C to 125°C		mA
			5.5	2.9	2.4		

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0 V \pm 10\%$ ,  $C_L = 50pF$ , Input  $t_r = t_f = 6.0 ns$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
$t_{PLH}, t_{PHL}$	Maximum Propagation Delay, Clock to $\bar{Q}$ or Q (Figures 1 and 4)	24	30	36	ns
$t_{PLH}, t_{PHL}$	Maximum Propagation Delay, Set or Reset to Q or $\bar{Q}$ (Figures 2 and 4)	24	30	36	ns
$t_{TLH}, t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
$C_{IN}$	Maximum Input Capacitance	10	10	10	pF
$C_{PD}$	Power Dissipation Capacitance (Per Enabled Output)	Typical @25°C, $V_{CC} = 5.0 V$			pF
	Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	130			

**TIMING REQUIREMENTS** ( $V_{CC} = 5.0 V \pm 10\%$ ,  $C_L = 50pF$ , Input  $t_r = t_f = 6.0 ns$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
$t_{su}$	Minimum Setup Time, Data to Clock (Figure 3)	15	19	22	ns
$t_h$	Minimum Hold Time, Clock to Data (Figure 3)	3	3	3	ns
$t_{rec}$	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	6	8	9	ns
$t_w$	Minimum Pulse Width, Clock (Figure 1)	15	19	22	ns
$t_w$	Minimum Pulse Width, Set or Reset (Figure 2)	15	19	22	ns
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

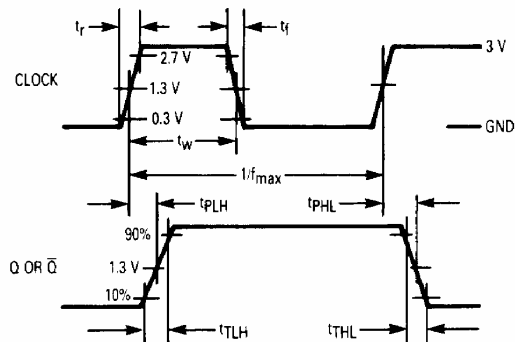


Figure 1. Switching Waveforms

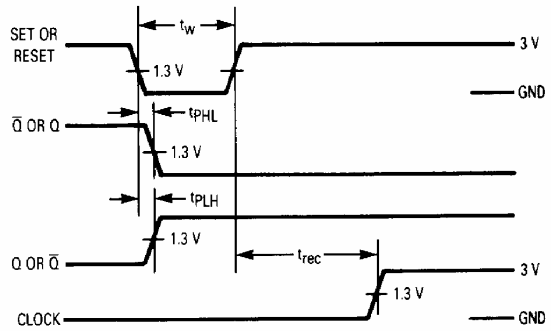


Figure 2. Switching Waveforms

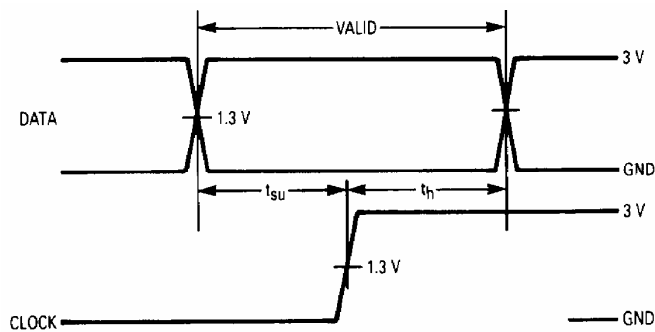
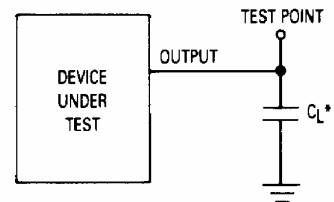


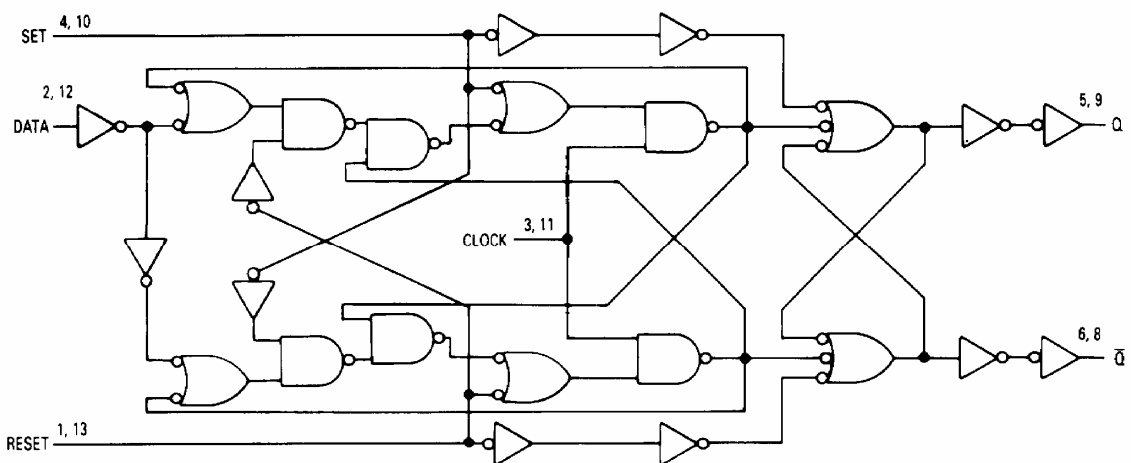
Figure 3. Switching Waveforms



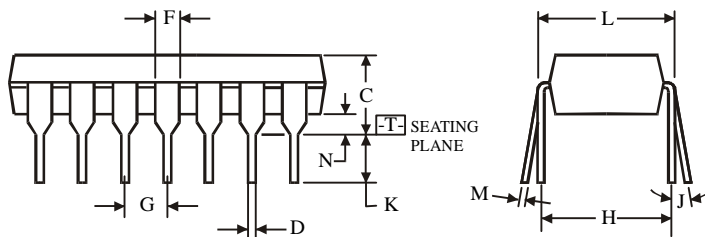
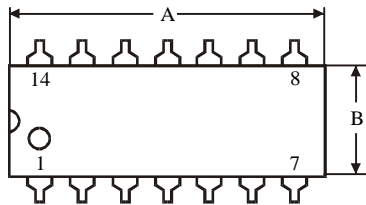
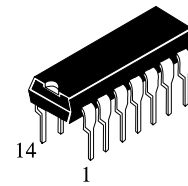
\*Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



**N SUFFIX PLASTIC DIP  
(MS - 001AA)**



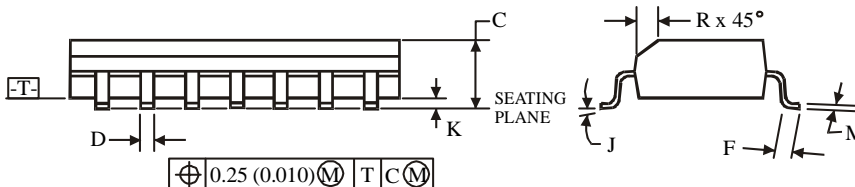
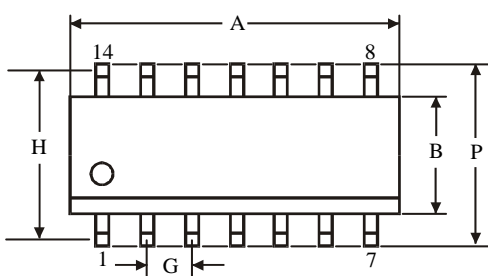
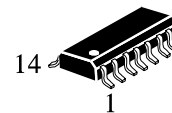
$\oplus 0.25 (0.010) \text{ (M) T}$

**NOTES:**

- Dimensions "A", "B" do not include mold flash or protrusions.  
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**D SUFFIX SOIC  
(MS - 012AB)**



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

**NOTES:**

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	8.55	8.75
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.27	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5