

5.0V/150mA Low-Drop Fixed-Voltage Regulator

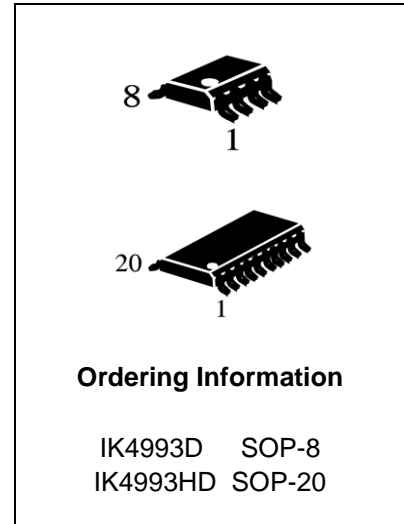
IK4993

GENERAL DESCRIPTION

The IK4993 is a monolithic integrated low-drop fixed voltage regulator 150mA with low current consumption.

The regulating output voltage element consists in a p-channel MOS and the regulation is performed regardless of input voltage transients up to 40V. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. The IK4993 is protected against short circuit and an over-temperature protection switches off the IC in case of extremely high power dissipation.

Reset and watchdog make this device particularly suitable to supply microprocessor systems in automotive applications.



FEATURES

- ◆ Operating DC supply voltage range 5.6V to 31V
- ◆ Output voltage tolerance: $\leq \pm 2\%$
- ◆ Low-drop voltage $\leq 400\text{mV}$
- ◆ Current capability up to 150mA
- ◆ Reset circuit sensing the output voltage down to 1V
- ◆ Programmable reset pulse delay with external capacitor
- ◆ Watchdog
- ◆ Programmable watchdog timer with external capacitor
- ◆ Enable input for enabling/disabling the watchdog functionality
- ◆ Thermal shutdown and short circuit protection
- ◆ T_j operation temperature -40 to +150°C
- ◆ Certified by AEC-Q100 standard

BLOCK DIAGRAM.

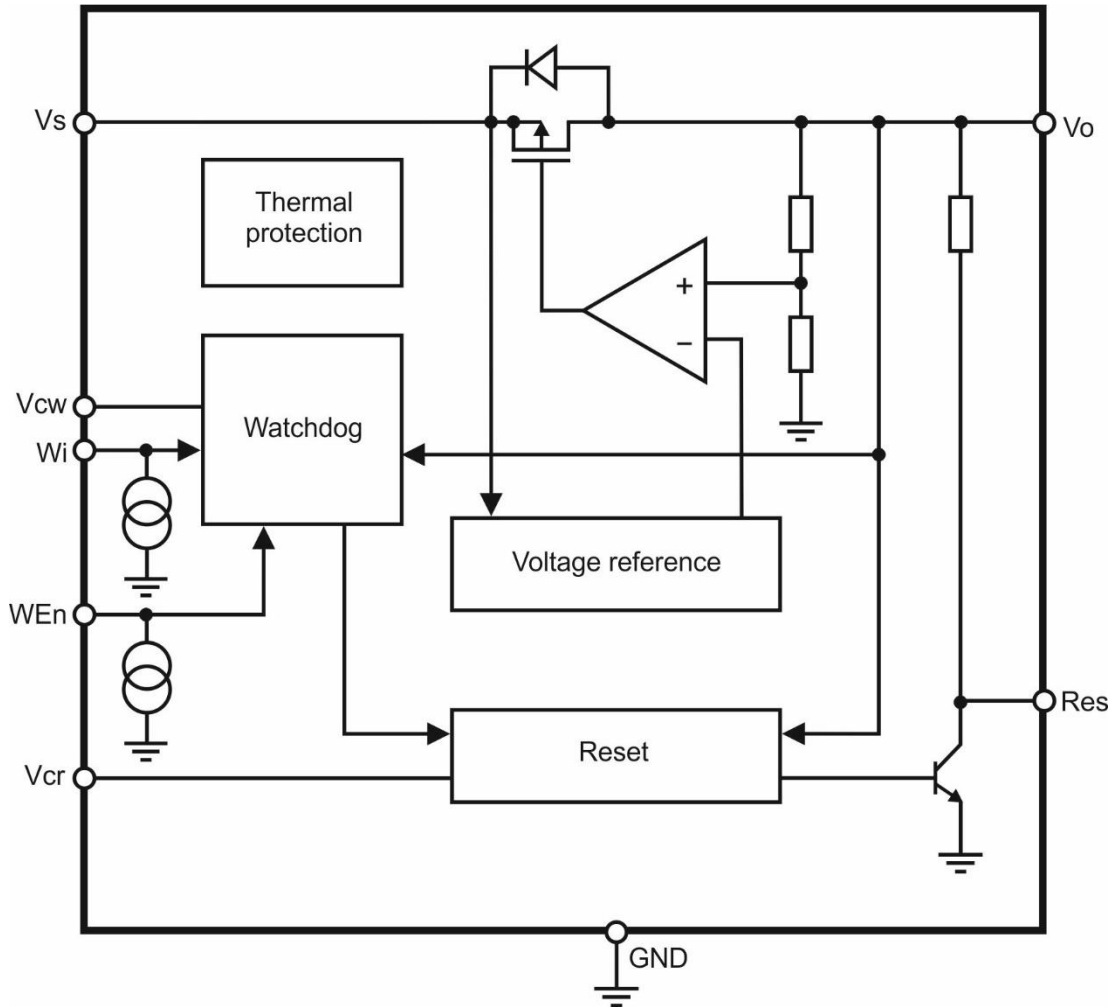


Fig. 1. Block diagram.

Table 1. PIN LIST AND DESCRIPTIONS.

Name	Pin (8 pin package)	Pin (20 pin package)	Description
WEn	1	1	Watchdog Enable input. If high watchdog functionality is active.
GND	2	4	Ground reference.
GND	-	5, 6, 15, 16	Ground. Connected these pins to a heat spreader ground.
Res	3	7	Reset output. It is pulled down when output voltage goes below V_{o_th} or frequency at W_i is too low. Leave floating if not used.
V_{CR}	4	10	Reset timing adjust. A capacitor between V_{CR} pin and GND, sets the reset delay time (trd).
V_{CW}	5	11	Watchdog timer adjust. A capacitor between V_{CW} pin and GND, sets the time response of the watchdog monitor.
W_i	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated. Connect to ground if not used.
V_o	7	17	Voltage regulator output. Block to ground with a capacitor >100nF (needed for regulator stability).
V_s	8	20	Supply voltage. Block to ground directly at IC pin with a capacitor.
N.C.	-	2, 3, 8, 9, 12, 13, 18, 19	Not connected.

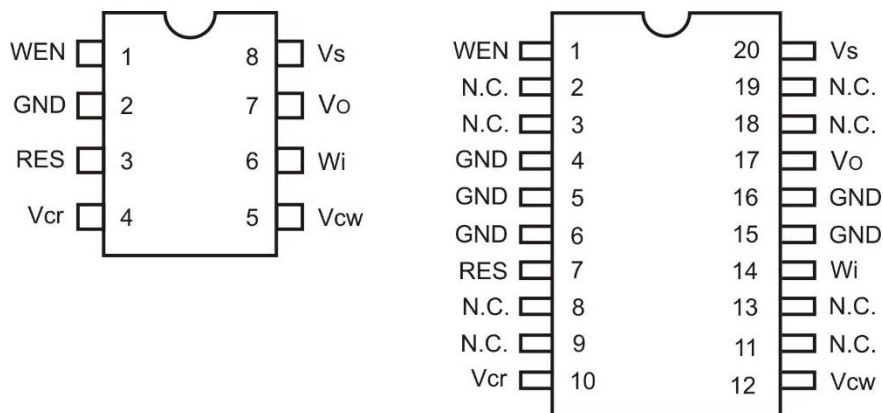


Fig. 2. Pins configuration.

Table 2. ABSOLUTE MAXIMUM RATINGS.T_j = - 40 to 150 °C

Symbol	Parameter	Value	Unit
V _S	DC supply voltage	-0.3 to 40	V
I _{VS}	Input current	Internally limited	
V _O	DC output voltage	-0.3 to 6	V
I _O	DC output current	Internally limited	
V _{WI}	Watchdog input voltage	-0.3 to V _O + 0.3	V
V _{OD}	Open drain output voltage	-0.3 to V _O + 0.3	V
I _{OD}	Open drain output current	Internally limited	
V _{CR}	Reset delay voltage	-0.3 to V _O + 0.3	V
V _{CW}	Watchdog delay voltage	-0.3 to V _O + 0.3	V
V _{WE_n}	Watchdog Enable input voltage	-0.3 to V _O + 0.3	V
T _j	Junction temperature	-40 to 150	°C
V _{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV
V _{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. THERMAL DATA.

Symbol	Parameter	Value	Unit
R _{th-jamb}	Thermal resistance Junction to Ambient: 8 pins package	130	°C/W
	20 pins package	51	°C/W

Note:

The values quoted are for PCB FR4 area = 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm, copper areas: SO-8= 2 cm², SO-20= 6 cm².

Electrical Characteristics.

Values specified in this section are for $V_s = 5.6V$ to $31V$, $T_j = -40^\circ C$ to $+150^\circ C$ unless otherwise stated.

Table 4. General parameters.

Pin	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_o	V_O	Output voltage	$V_s = 6$ to $31V$ $I_o = 1$ to $150mA$	4.9	5.0	5.1	V
V_o	I_{short}	Short circuit current	$V_s = 13.5V^{(1)}$	150	280	400	mA
V_o	$I_{lim}^{(2)}$	Output current limitation	$V_s = 13.5V^{(1)}$	150	320	500	mA
V_s, V_o	V_{line}	Line regulation voltage	$V_s = 6$ to $31V$ $I_o = 1$ or $150mA$			25	mV
V_o	V_{load}	Load regulation voltage	$I_o = 1$ to $150mA$ $V_s = 13.5V$			25	mV
V_s, V_o	$V_{dp}^{(3)}$	Drop voltage	$I_o = 150mA$		200	400	mV
V_s, V_o	SVR	Ripple rejection	$f_r = 100 Hz^{(4)}$	55			dB
V_s, V_o	I_{qn_150}	Quiescent current	$V_s=13.5V,$ $I_o=150mA,$ $WEn = high$		1.25	2	mA
V_s, V_o	I_{qn_50}	Quiescent current	$V_s=13.5V,$ $I_o=50mA,$ $WEn = high$		470	1000	μA
V_s, V_o	I_{qn_1}	Quiescent current	$V_s=13.5V,$ $I_o = 1mA,$ $WEn = high$		100	180	μA
V_s, V_o	I_{qs}	Quiescent current with watchdog regulator disabled	$V_s=13.5V,$ $I_o = 1mA,$ $WEn = low$		79	125	μA
	T_{jp}	Thermal protection temperature		150		190	$^\circ C$
	T_{jph}	Thermal protection temperature hysteresis			10		$^\circ C$

Note:

1. See Fig. 6.
2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at $V_s=13.5V$ and $I_o= 75mA$.
3. V_s-V_o measured when the output voltage has dropped 100mV from its nominal value obtained at $V_s=13.5V$ and $I_o= 75mA$.
4. Guaranteed by design.

Table 5. Reset output parameters.

Pin	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Res	V_{Res_l}	Reset output low voltage	$R_{ext} = 5k\Omega$ to V_o , $V_o > 1V$			0.4	V
Res	I_{Res_h}	Reset output high leakage current	$V_{Res} = 5V$			1	μA
Res	R_{p_u}	Pull up internal resistance	With respect to V_o	12	25	50	$k\Omega$
Res	V_o_th	V_o out of regulation threshold	$V_s = 6$ to $31V$, $I_o = 1$ to $150mA$	6%	8%	10%	Below V_o_ref
V_{CR}	V_{rlth}	Reset delay circuit low threshold	$V_s = 13.5V$	10%	13%	16%	V_o_ref
V_{CR}	V_{rhth}	Reset delay circuit high threshold	$V_s = 13.5V$	44%	47%	50%	V_o_ref
V_{CR}	I_{CR}	Charge current	$V_s = 13.5V$	8	17.6	30	μA
V_{CR}	I_{DR}	Discharge current	$V_s = 13.5V$	8	17.6	30	μA
Res	T_{rr_2}	Reset reaction time ⁽¹⁾	$V_o = V_o_th - 100mV$	100	275	1000	μs
Res	T_{rd}	Reset delay time	$V_s = 13.5V$, $C_{tr} = 1nF$	65		150	ms

Note:

When V_o becomes lower than 4V, the reset reaction time decreases down to $2\mu s$ assuring a faster reset condition in this particular case.

Table 6. Watchdog parameters.

Pin	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
W_i	V_{ih}	Input high voltage	$V_s = 13.5V$	3.5			V
W_i	V_{il}	Input low voltage	$V_s = 13.5V$			1.5	V
W_i	V_{ih_hyst}	Input hysteresis	$V_s = 13.5V$		500		mV
W_i	I_i	Pull down current	$V_s = 13.5V$		10	20	μA
V_{cw}	V_{whth}	High threshold	$V_s = 13.5V$	44%	47%	50%	V_o_ref
V_{cw}	V_{wlth}	Low threshold	$V_s = 13.5V$	10%	13%	16%	V_o_ref
V_{cw}	I_{cwc}	Charge current	$V_s = 13.5V$, $V_{cw} = 0.1V$	4	8	14	μA
V_{cw}	I_{cwd}	Discharge current	$V_s = 13.5V$, $V_{cw} = 2.5V$	1.0	2.13	4.5	μA
V_{cw}	T_{wop}	Watchdog period	$V_s = 13.5V$, $C_{tw} = 47nF$	25	50	90	ms
Res	t_{wol}	Watchdog output low time	$V_s = 13.5V$, $C_{tw} = 47nF$	6	10.5	22	ms

Table 7. Watchdog Enable parameters.

Pin	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
WEn	WEn_low	Enable input low voltage				1	V
WEn	WEn_high	Enable input high voltage		3			V
WEn	WEn_hyst	Enable input hysteresis		500	800	1100	mv
WEn	Ileak	Pull down current	WEn = 5V	2	8	20	μA

Test circuits.

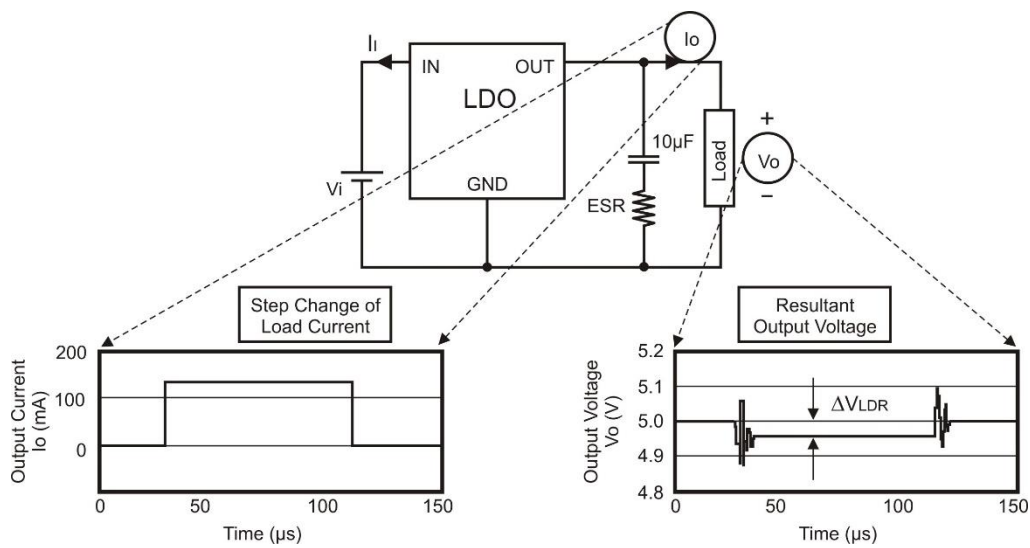


Fig. 3. Load regulation test circuit.

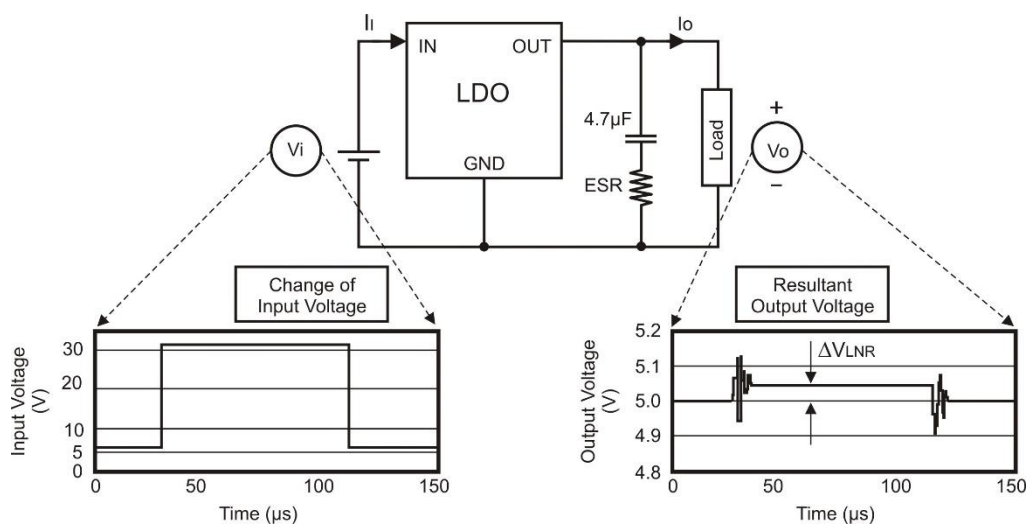


Fig. 4. Line regulation test circuit.

Application information.

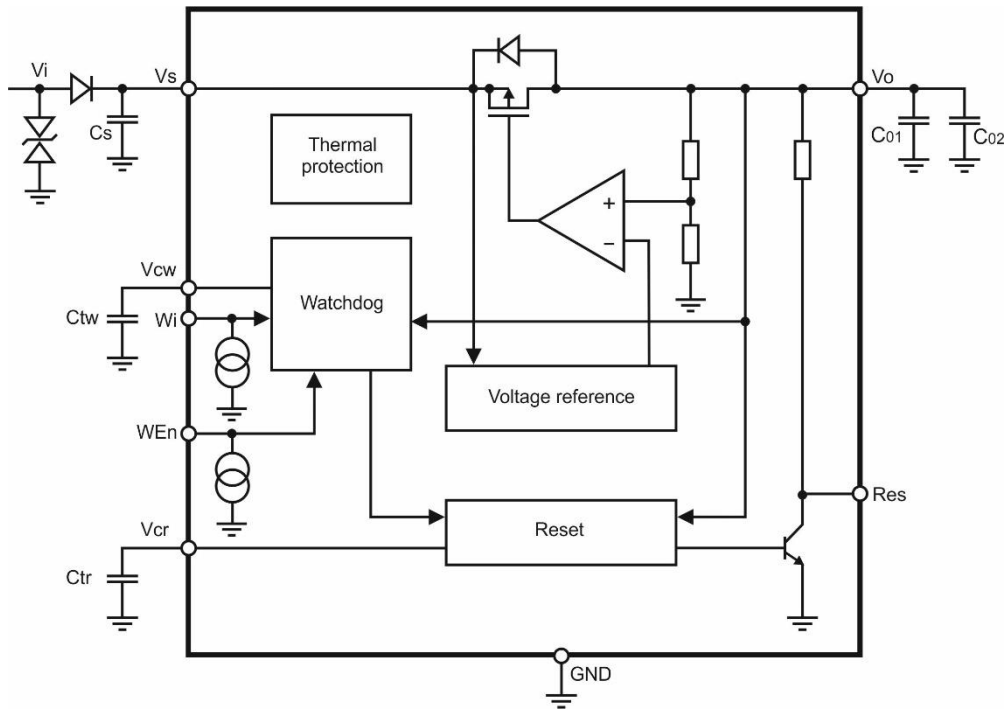


Fig. 5. Application circuit.

Voltage regulator.

Voltage regulator uses a p-channel transistor as a regulating element. With this structure, very low dropout voltage at current up to 500mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated.

A short circuit protection to GND is provided.

The voltage regulator watchdog functionality can be disabled by putting WEn low.

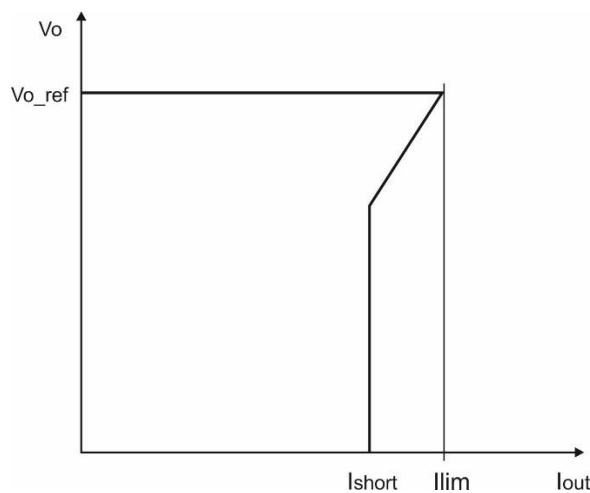


Fig. 6. Behavior of current limitation.

Reset.

The reset circuit supervises the output voltage V_o . The V_{o_th} reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than V_{o_th} then Res goes low with a reaction time t_{rr} . The reset low signal is guaranteed for an output voltage V_o greater than 1V. When the output voltage becomes higher than V_{o_th} then Res goes high with a delay t_{rd} . This delay is obtained by an internal oscillator.

The oscillator period is given by:

$$T_{osc} = [(V_{rhth}-V_{rlth}) \times C_{tr}] / I_{cr} + [(V_{rhth}-V_{rlth}) \times C_{tr}] / I_{dr}$$

where:

I_{CR} : is an internally generated charge current

I_{DR} : is an internally generated discharge current

V_{rhth} , V_{rlth} : two voltages defined with the output voltage and a resistor output divider.

C_{tr} : is an external capacitance.

t_{rd} is given by:

$$t_{rd} = 512 \times T_{osc}$$

Reset is active when En is high.

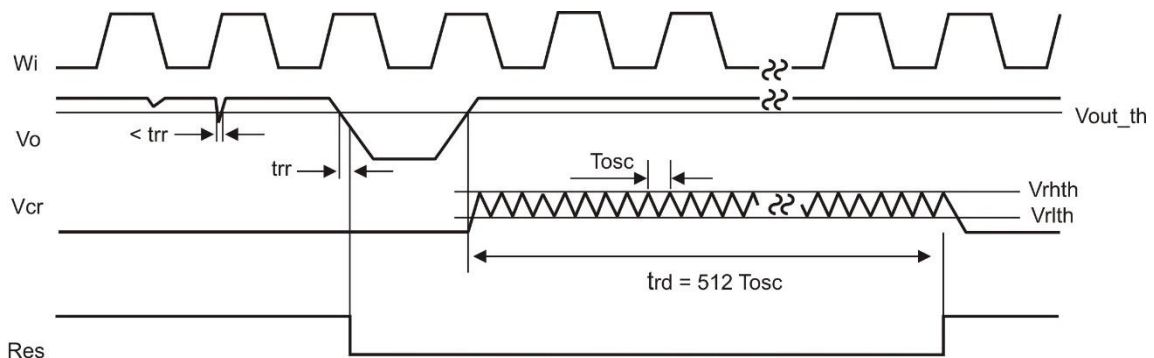


Fig. 7. Reset timing diagram.

Watchdog.

A connected microcontroller is monitored by the watchdog input Wi . If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, C_{tw} . The watchdog circuit discharges the capacitor C_{tw} , with the constant current I_{cwd} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth} . In order to calculate the minimum time t , during which the micro-controller must output the positive edge, the following equation can be used:

$$(V_{whth}-V_{wlth}) \times C_{tw} = I_{cwd} \times t$$

Every W_i positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, V_{wth} , the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor C_{tw} .

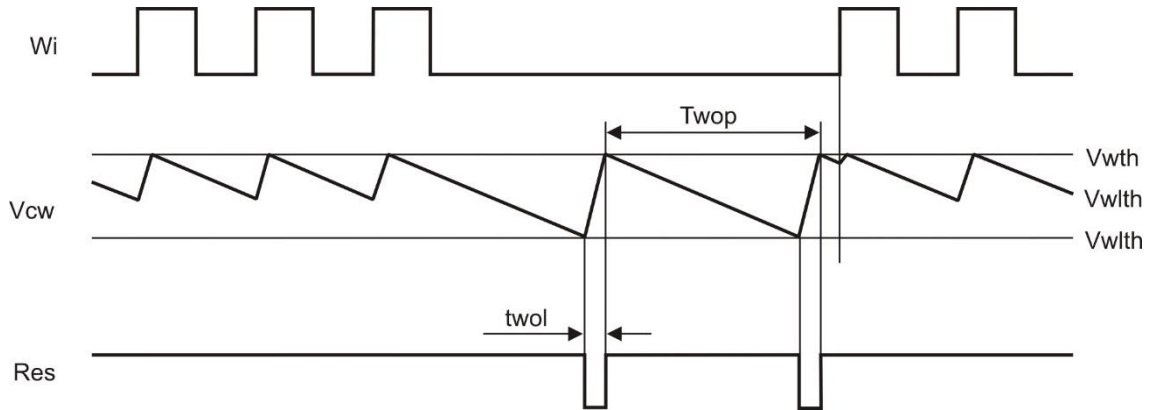


Fig. 8. The timing diagram of the watchdog.

Power Dissipation and Junction Temperature.

Most LDO regulators specify a junction temperature to assure their operations; the maximum junction temperature allowable without damaging the device is also specified. This restriction limits the power dissipation that the regulator can handle in any given application. To ensure that the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $PD (max)$, and the actual dissipation, PD , which must be less than or equal to $PD (max)$.

The maximum power dissipation limit is determined using the following equation:

$$PD (max) = T_{Jmax} - T_A / R_{JA}$$

Where

T_{Jmax} is the maximum allowable junction temperature.

R_{JA} is the thermal resistance junction-to-ambient for the package.

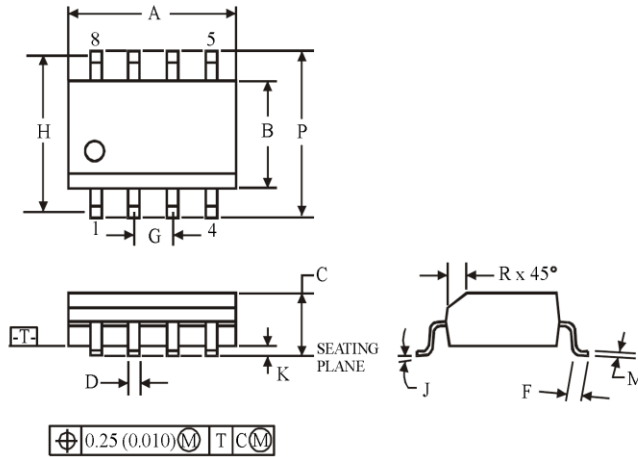
T_A is the ambient temperature.

The regulator power dissipation is calculated using:

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Package information.

D SUFFIX SOP
(MS - 012AA)

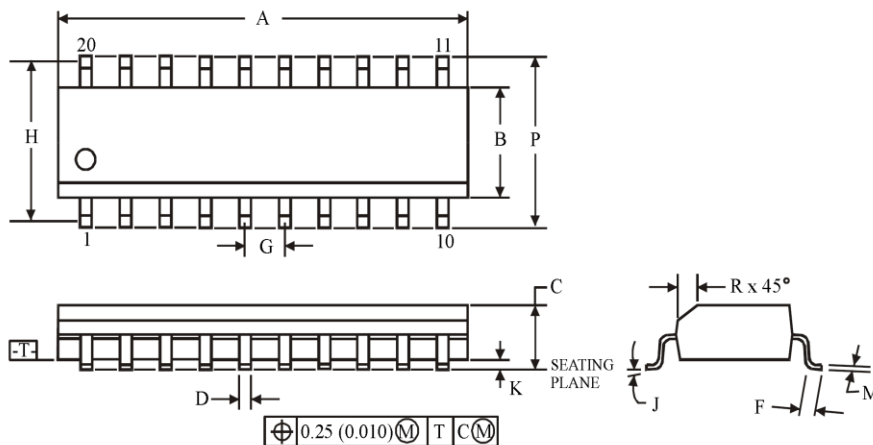
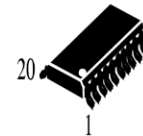


Symbol	Dimension, mm	
	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 013AC)



Symbol	Dimension, mm	
	MIN	MAX
A	12.60	13.00
B	7.40	7.60
C	2.35	2.65
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.10	0.30
M	0.23	0.32
P	10.00	10.65
R	0.25	0.75

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.