Active MOS FET Rectifier driver integrated circuit for alternator.

GENERAL DESCRIPTION

The IK8011 is an alternator active MOSFET rectifier driver IC. Specifically designed for Automotive applications.

Additional features of under and over voltage protections combine to make this design an extremely efficient and reliable device for use in Automotive applications.

FEATURES

- Direct connection to the gates of AMR
- Internal voltage regulator VDD
- Under-Voltage and Over-Voltage Lockout Protection by EEPROM set
- Over temperature protection (TJ > 160°C) by metal mask
- Ambient temperature range is - 40˚C to +150˚C
- AEC-Q-100 qualified

APPLICATIONS

AMR driver for alternators.

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Over temperature protection
IK8011	T_A = - 40°C +150°C	SOP16	absent
IK8011P	T_A = - 40°C +150°C	SOP16	present

Block Diagram.

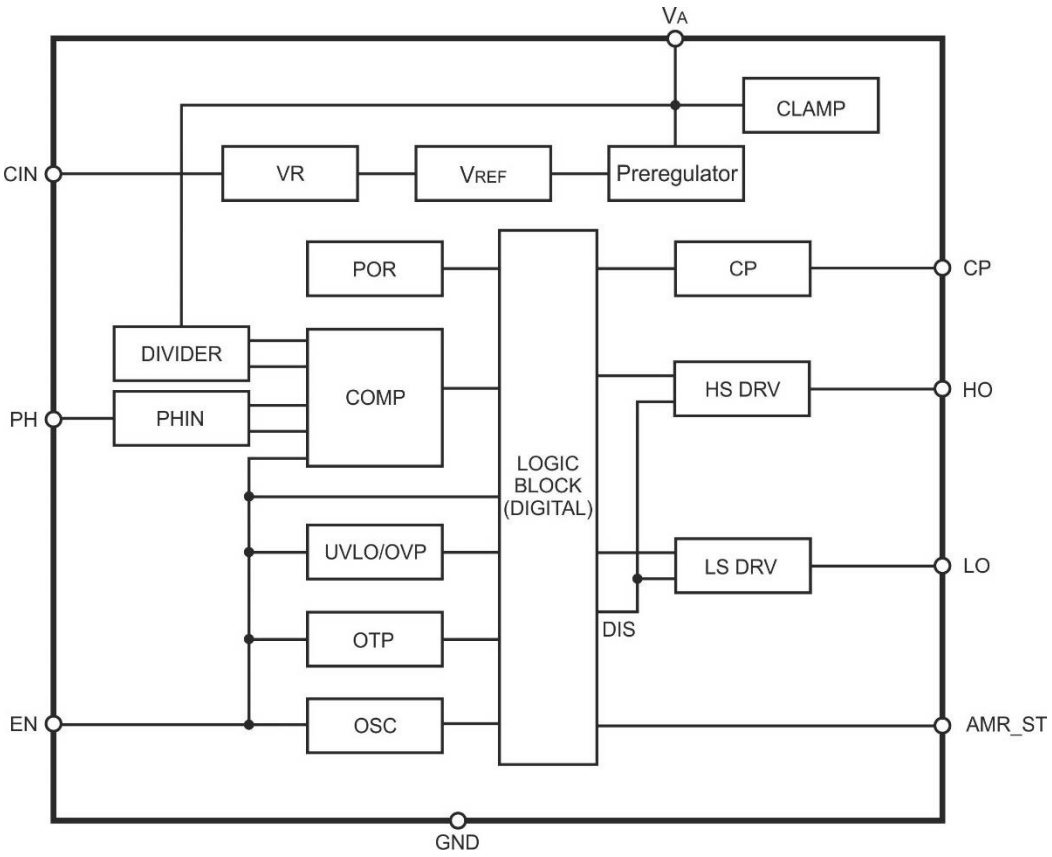


Fig. 1. Block diagram.

Pin Assignments.

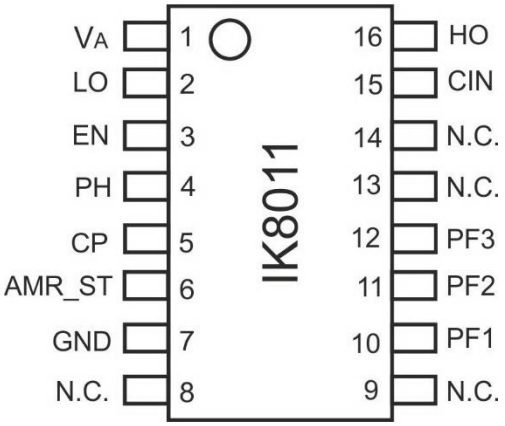


Fig.2. Pin assignments.

Table 1. PIN LIST AND DESCRIPTIONS.

Pin	Name	I/O	Description
1	V_A	P	Power supply pin.
2	LO	O	Low side MOSFET output pin.
3	EN	I	Enable signal input pin for test mode.
4	PH	I	Phase input pin.
5	CP	I	Charge pump capacitor input.
6	AMR_ST	O	AMR status output pin.
7	GND	P	Ground pin.
8	N.C.		Not contact
9	N.C.		Not contact
10	PF1	I	Trimming input pin.
11	PF2	I	Trimming input pin.
12	PF3	I	Trimming input pin.
13	N.C.		Not contact
14	N.C.		Not contact
15	CIN	I	Coupling VR block with capacitor.
16	HO	O	High side MOSFET output pin.

DESCRIPTIONS OF THE BLOCK DIAGRAM.

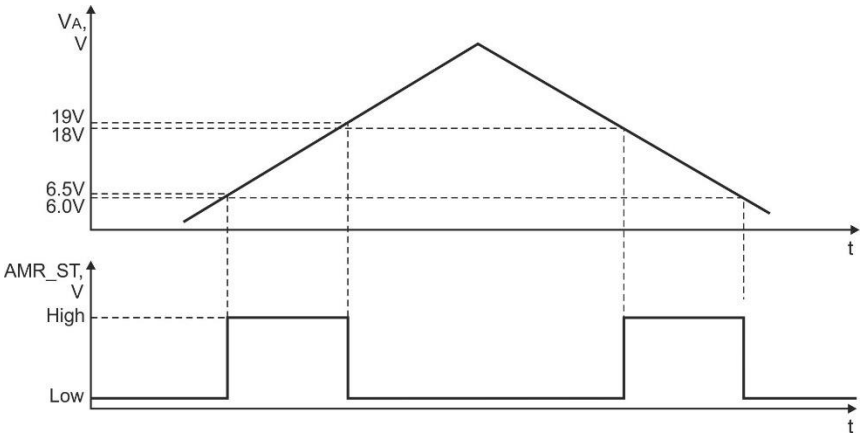


Fig. 3. AMR_ST function vs. V_A.

Table 2. AMR_ST function vs V_A (UVLO or OVP).

V_A	Event (UVLO or OVP). Disable mode.			Not event. Enable mode	
	Voltage level	State		Voltage level	State
HO	LOW relative to PH	High side TR	OFF	Any	Operation
		Low side TR	ON		
LO	LOW relative to GND	High side TR	OFF	Any	Operation
		LOW side TR	ON		
AMR_ST	LOW relative to GND	Operation		HIGH	Operation

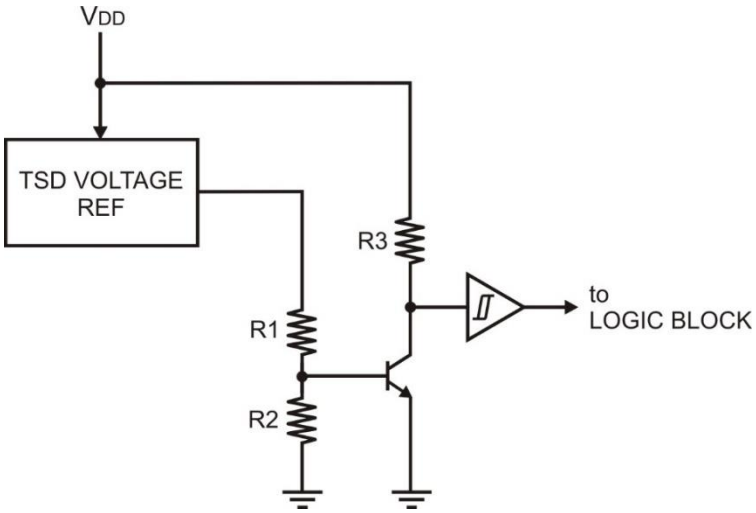


Fig. 4. Thermal shutdown block diagram.

Table 3. Thermal shutdown function.

TSD	Event (T_j >160°C). Disable mode.			Not event. Enable mode.	
	Voltage level	State		Voltage level	State
HO	LOW relative to PH	High side TR	OFF	Any	Operation
		Low side TR	ON		
LO	LOW relative to GND	High side TR	OFF	Any	Operation
		LOW side TR	ON		
AMR_ST	LOW relative to GND	Operation		HIGH	Operation

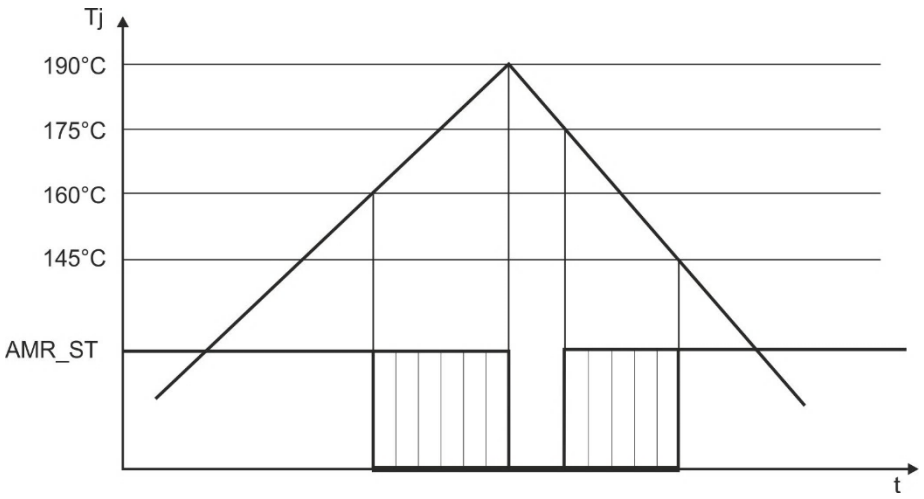


Fig. 5. TSD function

Table 5. EEPROM programming data.

Parameters	Symbol	Typical value	Trimming steps, mV		Remark
			minus	plus	
Threshold voltage for switch OFF the HO	V_{TH2H}	V_A	-5	+5	Total value from -75 mV till +75 mV
Threshold voltage for switch OFF the LO	V_{TH2L}	0	-5	+5	Total value from -75 mV till +75 mV

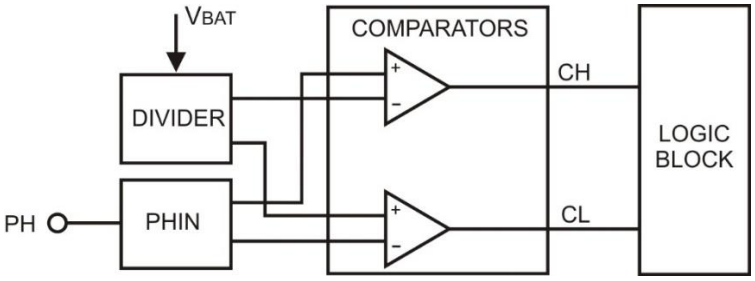


Fig. 6. Comparators block diagram connection.

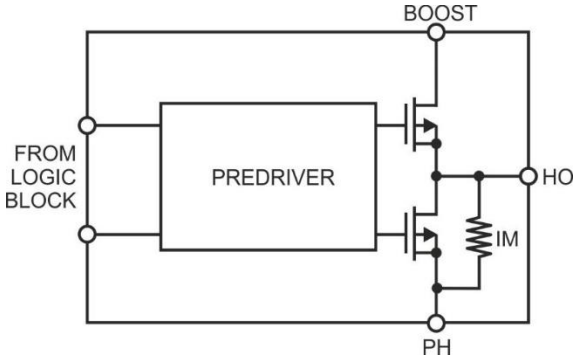


Fig. 7. High side driver block diagram.

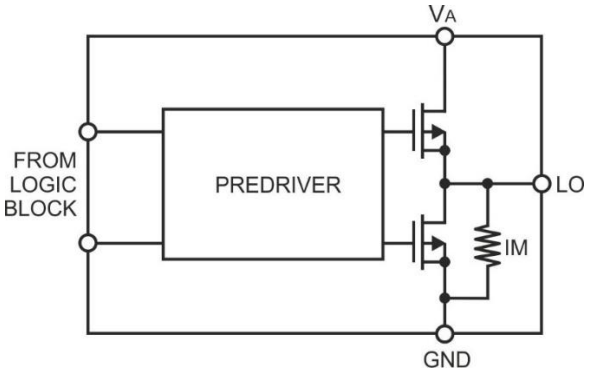


Fig. 8. Low side driver block diagram.

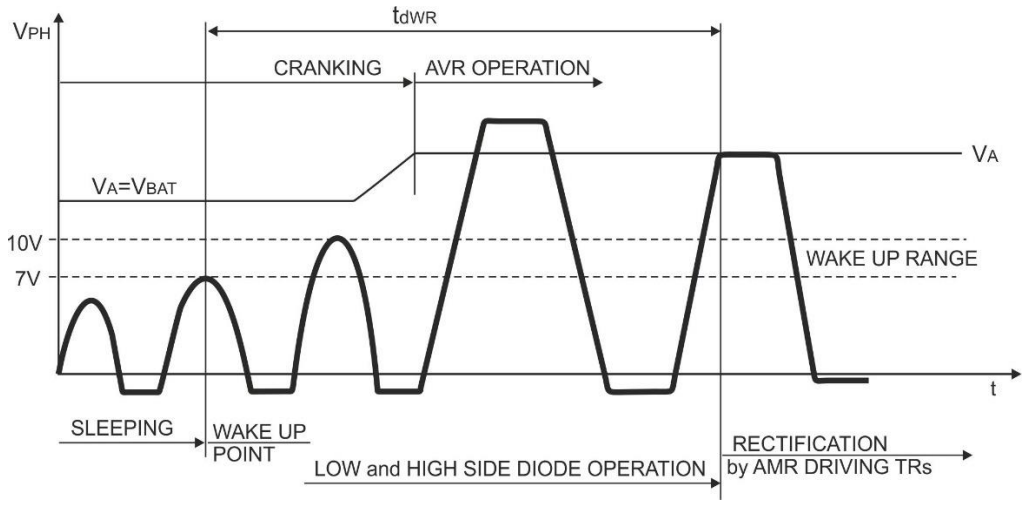


Fig. 9. Wake up process after sleeping mode.

When the cranking of engine started the phase voltage becomes higher. If phase voltage go in wake up range the IK8011 proceeds to rectification mode in t_{dWR} time (delay time from wake up to rectification between sleeping mode and rectification mode). During this t_{dWR} time the whole AMR blocks get power supply and start operation.

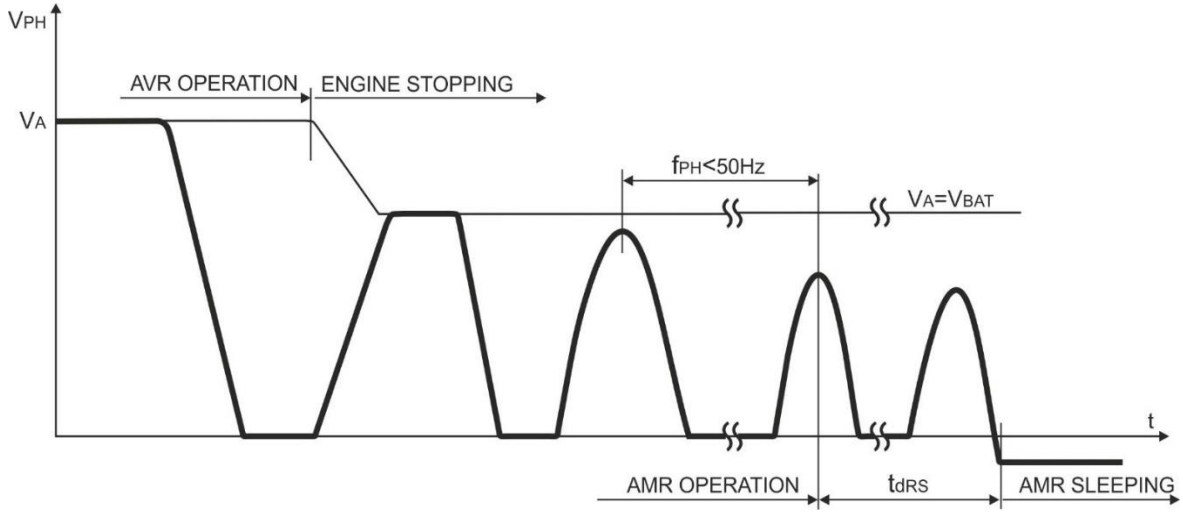


Fig. 10. Sleep ON process after rectification mode.

When the engine get stop the frequency of phase signal decreasing step by step. If this frequency drop out less 50±10Hz the AMR start the sleeping. In time t_{dRS} (delay time from rectification mode to sleeping mode) the IK8011 start sleep and whole AMR blocks switch OFF from power supply line.

Table 6. ABSOLUTE MAXIMUM RATINGS.

Unless otherwise specified, all voltages are referred to V_{SS}. Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. TA=25°C unless otherwise specified.

Symbol	Parameter	Value		Unit
		Min	Max	
V_A	DC supply voltage (any time)	-0.3	40	V
V_{INPH}	PH input voltage	V_{GND} – 0.5	40.0	V
V_{INC}	Input voltage on CIN pin	V_{GND} – 0.3	6.0	V
V_{INCP}	Input voltage on CP pin	V_{GND} – 0.3	20.0	V
V_{EN}	Input voltage on EN pin	V_{GND} – 0.3	5.75	V
V_{OUTHO}	HO output voltage	V_{GND} – 0.3	40	V
V_{OUTLO}	LO output voltage	V_{GND} – 0.3	20	V
V_{OUT1}	V_{AMR_ST} pin output voltage	V_{GND} – 0.3	5.75	V
Tstg	Storage Temperature	-55	150	˚C
T_J	Junction Temperature	-40	160	˚C
Tamb	Ambient Temperature	-40	150	˚C
ESD	ESD HBM		8	kV
	ESD CDM		750	V
	ESD MM		200	V

Notes:
1. Revers voltage protection by external device.

Table 7. RECOMMENDED OPERATING RANGE.

Unless otherwise specified, all voltages are referred to V_{SS}.

Symbol	Parameter	Value		Unit
		Min	Max	
V_A	DC supply voltage	6	18	V
V_{INPH}	PH input voltage	-0.2	18	V
V_{EN}	EN input voltage	0	5.5	V
V_{INC}	Input voltage on CIN pin	0	5.5	V
V_{INCP}	Input voltage on CP pin	6	18	V
V_{OUTHO}	HO output voltage	0	30	V
V_{OUTLO}	LO output voltage	0	18	V
V_{OUT1}	AMR_ST output voltage	0	5.5	V
Tj	Junction Temperature	-40	150	˚C
Tamb	Ambient Temperature	-40	150	˚C

Table 8. Electrical Characteristics.

T_A=T_{OP}=+25˚C. All voltages are defined with respect to ground. Positive currents flow into the device. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pins V_A, V_{DD} (CIN)						
V_A	Operating voltage		6.0	12.0	18.0	V
V_{DD}	Voltage regulator output reference voltage	V_A =12.0 V	4.5	5.0	5.5	V
I_{STBY}	Stand-by current	V_A =12.0V, V_{PH} = 0V, f_{PH} = 0Hz	-	2	10	uA
UVLO & OVP						
V_{OVP_ON}	Over voltage protection ON (rump up)	V_A rump up	18.3	19.0	20.0	V
V_{OVP_OFF}	Over voltage protection OFF (rump down)	V_A rump down	17.3	18.0	19.0	V
V_{OVPHYS}	Over voltage protection hysteresis		0.6	1.0	1.4	V
V_{UV-OFF}	Under-voltage lock-out OFF (rump up)	V_A rump up	6.1	6.5	6.9	V
V_{UV-ON}	Under-voltage lock-out ON (rump down)	V_A rump down	5.6	6.0	6.4	V
V_{UV-HYS}	Under-voltage lock-out hysteresis*		0.3	0.5	0.7	V
EN pin						
V_{ENH}	EN input high level voltage (test mode)	V_A= 12V	0.8	1.1	2.0	V
V_{ENL}	EN input low level voltage (operation mode)	V_A= 12V	0.5	0.9	1.5	V
AMR_ST pin (open drain)						
V_{AMRSTL}	Low output voltage of V_{AMR_ST} signal	V_A= 12V, I_{SINK} = 0 to 2mA	0	0.1	1.0	V
TSD block						
T_{TSD}	Thermal shut down temperature*	V_A = 12V	160	175	190	°C
T_{TSDHYS}	Thermal shut down hysteresis*	V_A = 12V	- 15	-	+15	°C

Table 8. Electrical Characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PH pin						
V_{TH1H}	Threshold voltage for switch ON the HO	V_A = 14V	V_A	V_A +0.05	V_A +0.2	V
V_{TH2H}	Threshold voltage for switch OFF the HO	V_A = 14V	V_A	V_A +0.05	V_A +0.1	V
V_{TH1L}	Threshold voltage for switch ON the LO	V_A = 14V	- 0.2	- 0.05	0.0	V
V_{TH2L}	Threshold voltage for switch ON the LO	V_A = 14V	-0.1	- 0.05	0	V
VPH_{AMR}	AMR start rectification threshold	V_A = 14V, $V_{EN} = V_{ENH}$,	-	-	$V_{PH} \geq V_A$	
VPH_{WR}	Phase voltage threshold for wake up process	V_A = 12V	7.0	8.5	10.0	V
t_{dWR}	Delay time from wake up to rectification between sleeping mode and rectification mode*	V_A = 12V	5	35	100	ms
fPH_{RS}	Phase frequency for sleeping ON process*	V_A = 12V	40	50	60	Hz
t_{dRS}	Delay time from rectification mode to sleeping mode*	V_A = 12V	20	100	200	ms
HALF bridge						
$I_{HB\ LCUR}$	Pulse loading current for low side Rectifier gate *	V_A = 12.0V	0.5			A
V_{OHLS}	Drop out voltage for low side Rectifier gate driver	V_A =12.0V, I_{LOAD} = - 100mA	0.4	0.90	1.5	V
V_{OLLS}	Output voltage for low side Rectifier gate driver	V_A =12.0V, I_{LOAD} = 100mA	0.1	0.5	1.0	V
t_{RL}	Rising time for low side driver*	V_A =12.0V C_{LOAD} = 12.0 nF	100	230	350	ns
t_{FL}	Falling time for low side driver*	V_A =12.0V C_{LOAD} = 12.0 nF	100	200	350	ns
$I_{HB\ HCUR}$	Pulse loading current for high side Rectifier gate *	V_A =12.0V	0.5			A
V_{OHHS}	Drop out voltage for high side Rectifier gate	V_A =12.0V, I_{LOAD} = - 100mA	0.1	0.5	1.0	V
V_{OLHS}	Output voltage for high side Rectifier gate	V_A =12.0V, I_{LOAD} = 100mA	0.1	0.5	1.0	V

Table 8. Electrical Characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HALF bridge						
t_{RH}	Rising time for high side driver*	V_A =12.0V C_{LOAD} = 12.0 nF	100	200	350	ns
t_{FH}	Falling time for high side driver*	V_A =12.0V C_{LOAD} = 12.0 nF	50	140	250	ns
td1	Delay time for half bridge HO driver switch ON *	V_A =12.0V	1.0	6.0	10.0	us
td2	Delay time for half bridge HO driver switch OFF *	V_A =12.0V	0.1	0.8	5.0	us
td3	Delay time for half bridge LO driver switch ON *	V_A =12.0V	1.0	6.0	10.0	us
td4	Delay time for half bridge LO driver switch OFF *	V_A =12.0V,	0.1	0.8	5.0	us

Note:
1. * Guarantee by design.

Application Notes.

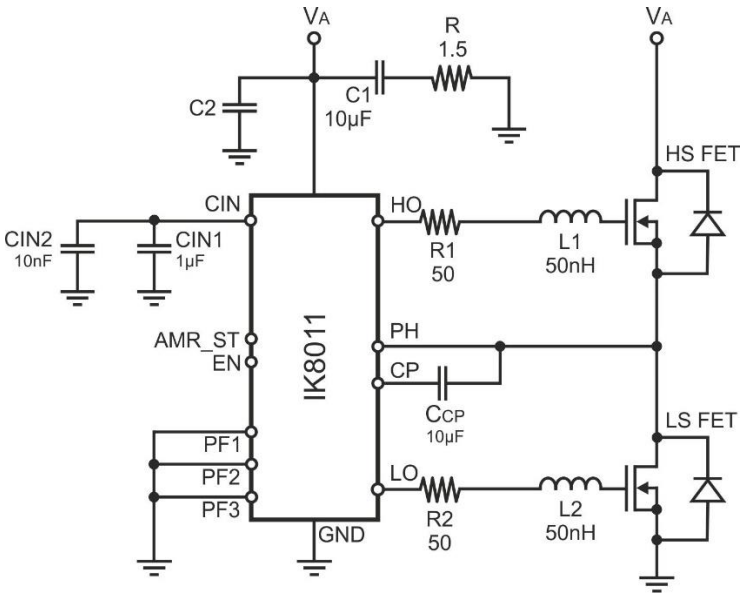


Fig. 12. Application circuit schematic for Half bridge connection (for protected MOS FET – 22 V<V_{BRDS} < 27 V).

Note: 1. IK8011 start rectification after fulfil condition: $V_{PH} > V_A$.

2. Customer can connect pins AMR_ST and EN to GND line in case of their requirement.

3. R1, R2 value are from 5.6 Ω till 200 Ω – depend on customer evaluation results.

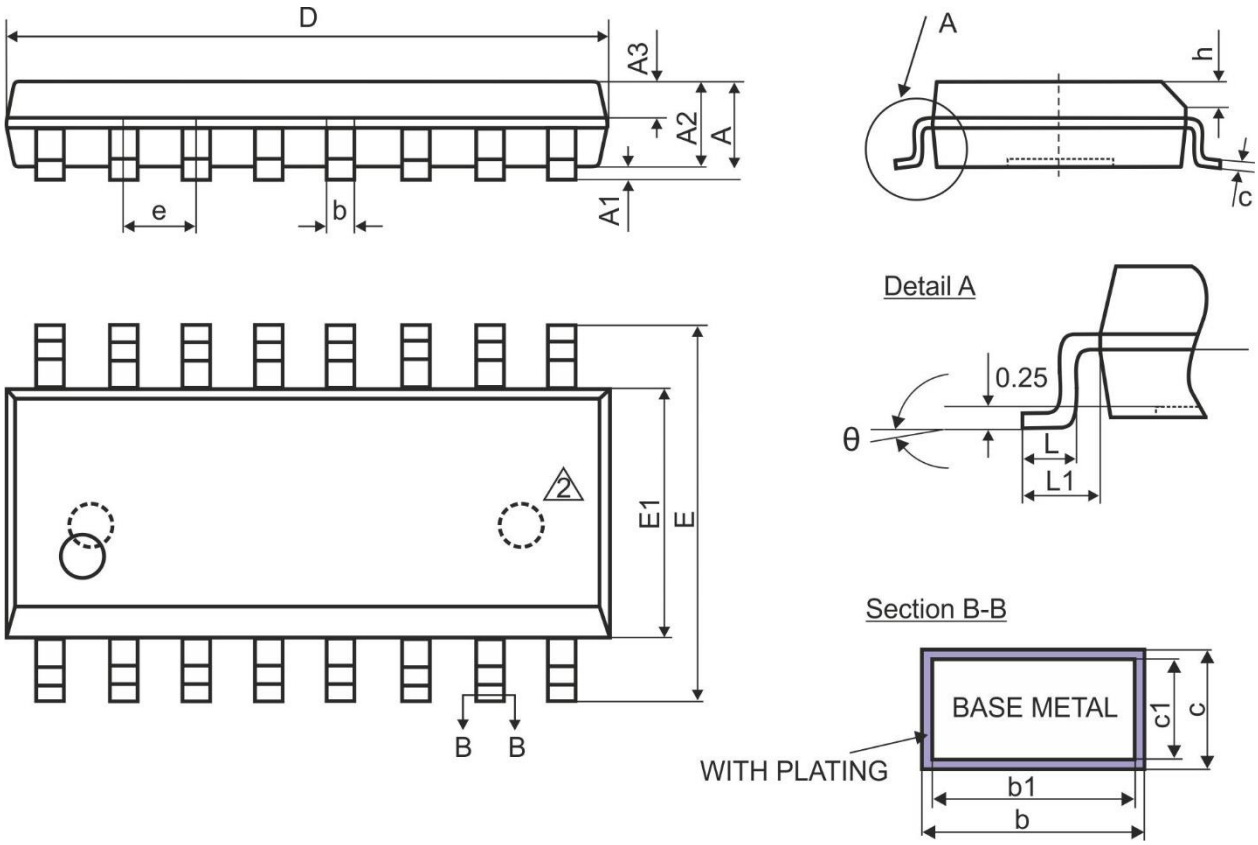
4. CP is 10.0 uF.

5. C2 value for RE test adjustable.

6. L1 and L2 will final customer decision under MOS FET right operation condition.

Package dimensions.

SOP 16.



Symbol	Millimeters		
	min	nom	max
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05		
Θ	0	-	8°

Revisions history

Date	Revision	Changes	Remark
15.04.2015	0.0	Initial release	
27.04.2015	0.01	1. Page 1. Changed the name of IC. Inserted junction and ambient temperatures. 2. Page 2. Renew the block diagram. 3. Page 4. Table 1 changed. 4. Page 5. Fig. 4 and Table 2 changed. 5. Page 6. Table 3 changed, Fig. 5, 6, 7 inserted. 6. Page 7. Fig. 8 inserted. 7. Page 8. Table 4 changed. 8. Page 9. Table 5 changed. 9. Page 9, 10, 11. Table 6 changed.	
17.08.2015	0.02	1. Page 2. Fig. 1 block diagram renew. 2. Page 4. Table 2. Pin assignment changed. 3. Page 7. Fig.6. Added new. 4. Page 7. Fig. 7. HO block diagram changed. 5. Page 8. Table 4. Changed according Block diagram. 6. Page 9. Table 5. Changed according Block diagram. 7. Page 9. Table 6. Inserted the V_{DD} value. 8. Page 10. Table 6. Changed. 9. Page 12. Fig. 5. Changed. 10. Page 12. Fig. 6. Changed.	
19.04.2016	0.03	1. Page 1. Package form – bare chip. 2. Page 2. Block diagram – updated. 3. Page 4. Table 1. Updated. 4. Page 5 – 11. Updated	
11.05.2016	0.04	All pages updated – see yellow color.	
15.06.2016	0.05	1. Page 1 – package changed for SOP-14. 2. Page 4. Fig.5. Changed. 3. Page 7. Table 4, 5. T_A changed. 4. Page 8. T_{SD} changed. 5. Page 9. $VPH_{AMR,}$ $VPH_{LDH,}$ VPH_{LDL} insert. 6. Page 13. SOP-14 package insert.	
24.06.2016	0.06	1. Page 2, 3. Changed pin assignment. 2. Page 4. TSD changed. 3. Page 7. T_J changed. 4. Page 8. Table 6. I_{STBY} changed.	
5.07.2016	0.07	1. Page 7. Fig. 11 and 12 inserted. 2. Page 10. Table 6. Updated for wake up and sleeping process.	
4.08.2016	0.08	1. Page 3. Table 2. Updated. 2. Page 4. Table 3. Updated. 3. Page 5. New Table 4 inserted (Load Dump mode). 4. Page 6. Fig.7, 8. Inserted the 1M resistors 5. Page 9. Table 8. I_{STBY} changed.	
8.08.2016	0.09	1. Page 5. Table 5 inserted. 2. Page 11. Table 8. Updated.	

Date	Revision	Changes	Remark
27.04.2017	0.10	1. Page 1. T_J > 160°C. 2. Page 4. T_J > 160°C. 3. Page 4. Fig. 5. Renew. 4. Page 5. Table 5. Thresholds renew, remove td2H,td2L; inserted t_{dtH} and t_{dtL}. 5. Page 6. Fig. 7. Inserted new one. 6. Page 7. Fig. 10. Renew. 7. Page 7. Fig 11. Remove. 8. Page 8. Table 6. T_J, ESD HBM CP pin inserted. 9. Page 9. Table 8. OVP limits changed. 10. Page 10. Table 8. Parameter limits changed. 11. Page 11. Table 8. Parameter limits changed. 12. Page 12. Fig 13. Renew.	All changes marked by yellow
22.08.2017	0.11	Change SOP14 for SOP16.	
14.12.2017	0.12	All pages upgraded.	Changes marked by yellow
23.05.2018	0.13	All pages updated by customer requirement	