

IW4019B

Quad AND/OR Select Gate
High-Voltage Silicon-Gate CMOS

The IW4019B types consist of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input gate. Selection is accomplished by control bits S_a and S_b . In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function

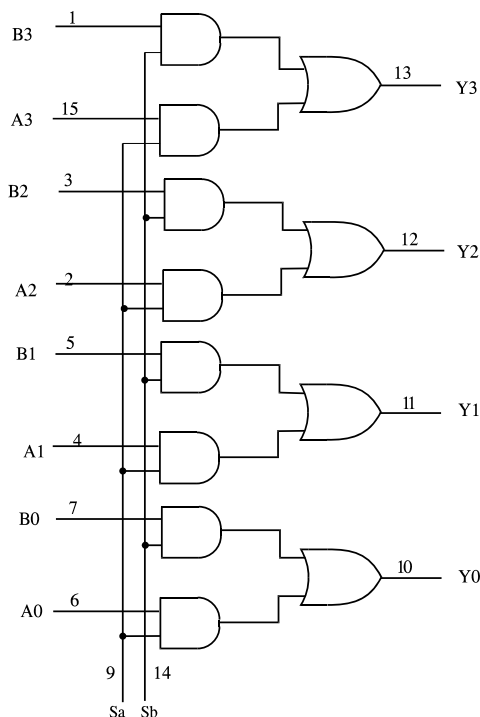
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply

N SUFFIX PLASTIC

DW SUFFIX SOIC

ORDERING INFORMATION
 IW4019BN Plastic
 IW4019BDW SOIC
 $T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN 16 = V_{CC}
 PIN 8 = GND

PIN ASSIGNMENT

B3	1	16	V_{CC}
A2	2	15	A3
B2	3	14	S_b
A1	4	13	Y3
B1	5	12	Y2
A0	6	11	Y1
B0	7	10	Y0
GND	8	9	S_a

FUNCTION TABLE

Inputs				Outputs
S_a	S_b	A	B	Y
H	L	H	X	H
H	L	L	X	L
L	H	X	H	H
L	H	X	L	L
L	L	X	X	L
H	H	L	L	L
H	H	L	H	H
H	H	H	L	H
H	H	H	H	H

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P _D	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5V or V _{CC} - 0.5V V _{OUT} =1.0V or V _{CC} - 1.0V V _{OUT} =1.5V or V _{CC} - 1.5V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.5V or V _{CC} - 0.5V V _{OUT} =1.0V or V _{CC} - 1.0V V _{OUT} =1.5V or V _{CC} - 1.5V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	1	1	30	μA
			10	2	2	60	
			15	4	4	120	
			20	20	20	600	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2.0	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, $R_L=200\text{K}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A, B, S_A or S_b to Output Y (Figure 1)	5.0	300	300	600	ns
		10	120	120	240	
		15	100	100	200	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
C_{IN}	Maximum Input Capacitance	All A and B Inputs	-		7.5	pF
		S_a and S_b Inputs	-		15.0	pF

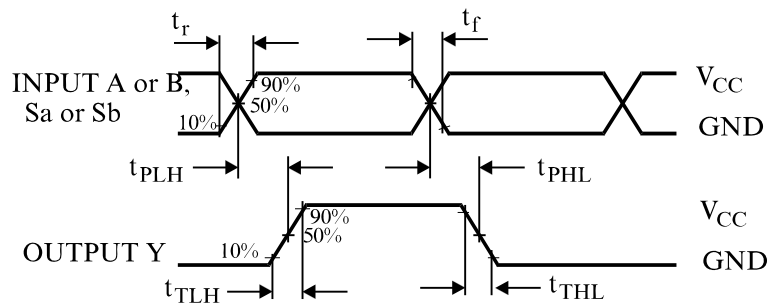
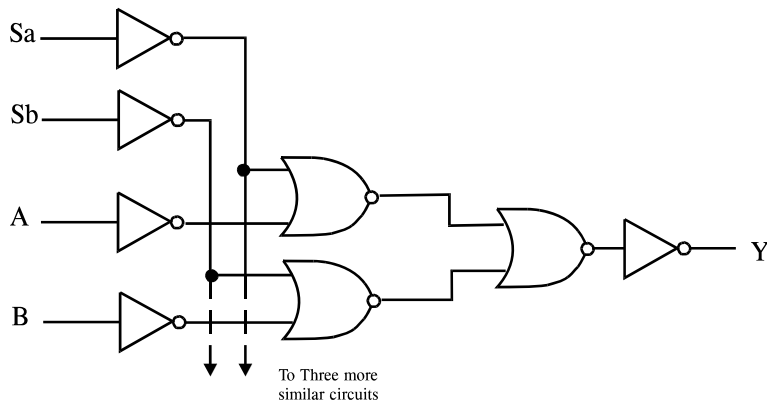
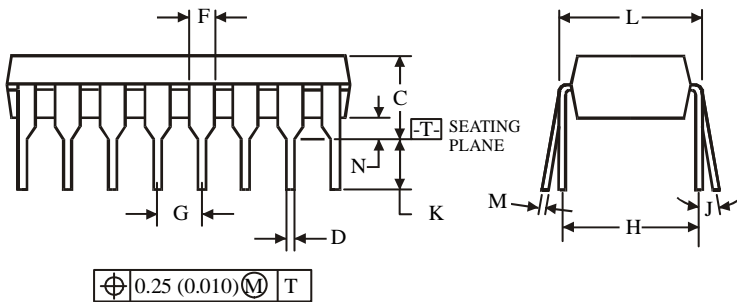
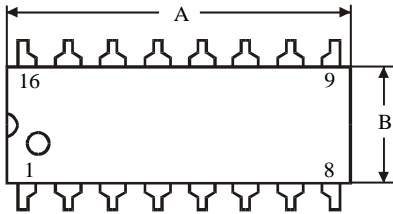
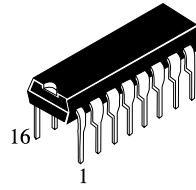


Figure 1. Switching Waveforms

EXPANDED LOGIC DIAGRAM
(1/4 of the Device)



**N SUFFIX PLASTIC
(MS - 001BB)**

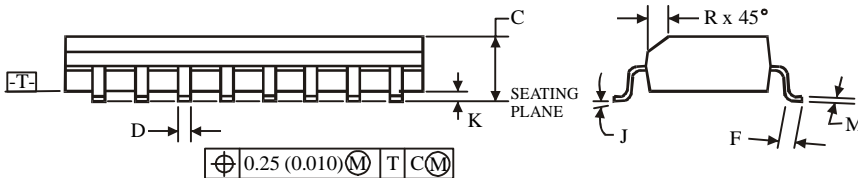
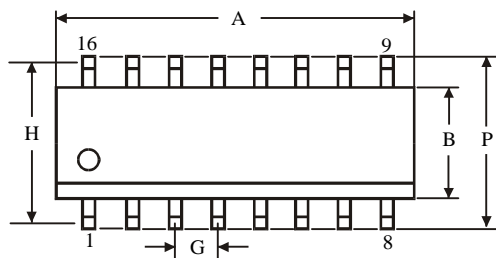
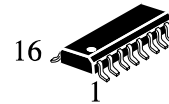


Symbol	Dimensions, mm	
	MIN	MAX
A	18.67	19.69
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions. Maximum mold flash or protrusions 0.25 mm (0.010) per side.

**D SUFFIX SOIC
(MS - 012AC)**



Symbol	Dimensions, mm	
	MIN	MAX
A	9.80	10.0
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A, for B - 0.25 mm (0.010) per side.