

**IW4034B**

**8-Stage Static Bidirectional Parallel/  
Serial Input/Output Bus Register  
High-Voltage Silicon-Gate CMOS**

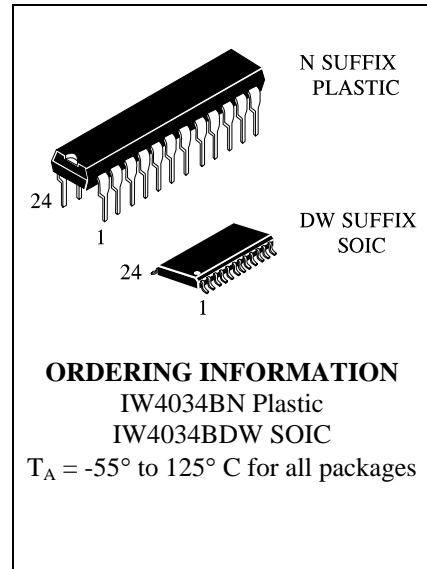
The IW4034B is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/ B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

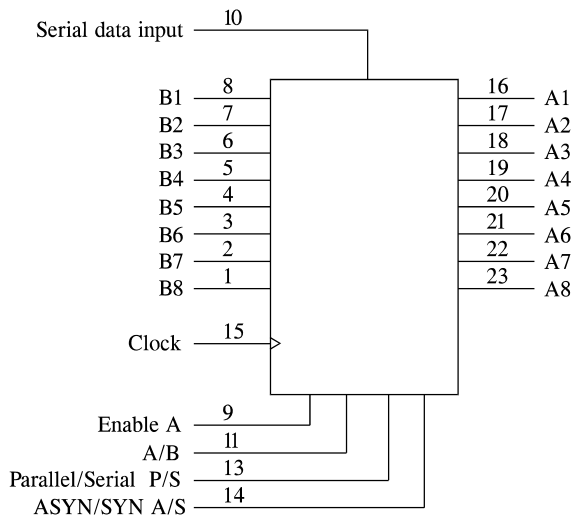
Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (3-state outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10.0 V supply
  - 2.5 V min @ 15.0 V supply

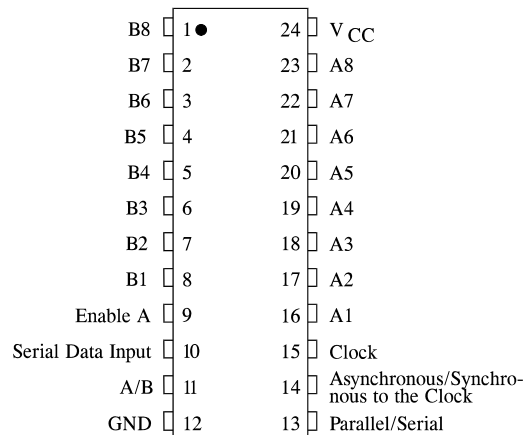


**LOGIC DIAGRAM**



PIN 24= $V_{CC}$   
 PIN 12= GND

**PIN ASSIGNMENT**



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P <sub>D</sub>	Power Dissipation per Output Transistor	100	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	3.0	18	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> = 0.5 V or V <sub>CC</sub> - 0.5V V <sub>OUT</sub> = 1.0 V or V <sub>CC</sub> - 1.0 V V <sub>OUT</sub> = 1.5 V V <sub>CC</sub> - 1.5V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> = 0.5 V or V <sub>CC</sub> - 0.5V V <sub>OUT</sub> = 1.0 V or V <sub>CC</sub> - 1.0 V V <sub>OUT</sub> = 1.5 V V <sub>CC</sub> - 1.5V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = GND or V <sub>CC</sub>	18	±0.1	±0.1	±1.0	μA
I <sub>OZ</sub>	Minimum Three State Leakage Current	Output in High-Impedance State V <sub>IN</sub> = GND or V <sub>CC</sub> V <sub>OUT</sub> = GND or V <sub>CC</sub>	18	±0.4	±0.4	±12.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = GND or V <sub>CC</sub>	5.0	5	5	150	μA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I <sub>OL</sub>	Minimum Output Low (Sink) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> U <sub>OL</sub> =0.4 V U <sub>OL</sub> =0.5 V U <sub>OL</sub> =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I <sub>OH</sub>	Minimum Output High (Source) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> U <sub>OH</sub> =2.5 V U <sub>OH</sub> =4.6 V U <sub>OH</sub> =9.5 V U <sub>OH</sub> =13.5 V	5.0	-2	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

**AC ELECTRICAL CHARACTERISTICS** ( $C_L=50\text{pF}$ ,  $R_L=200\text{k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$f_{\text{max}}$	Maximum Clock Frequency (Figure 2)	5.0	2	2	1	MHz
		10	5	5	2.5	
		15	7	7	3.5	
$t_{\text{PHL}}$ , $t_{\text{PLH}}$	Maximum Propagation Delay, A(B) Parallel Data In to B(A) Parallel Data Out; Serial to Parallel Data Out (Figures 1,2)	5.0	700	700	1400	ns
		10	240	240	480	
		15	170	170	340	
$t_{\text{PLZ}}$ , $t_{\text{PHZ}}$ , $t_{\text{PZL}}$ , $t_{\text{PZH}}$	Maximum Propagation Delay, A/B or AE to "A" Output (Figure 3)	5.0	400	400	800	ns
		10	160	160	320	
		15	120	120	240	
$t_{\text{THL}}$ , $t_{\text{TLH}}$	Maximum Output Transition Time, Any Output (Figures 1,2)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
$C_{\text{IN}}$	Maximum Input Capacitance	-		7.5		pF

**TIMING REQUIREMENTS** ( $C_L=50\text{pF}$ ,  $R_L=200\text{ k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$t_{\text{su}}$	Minimum Setup Time, Serial Data to Clock (Figure 4)	5.0	160	160	320	ns
		10	60	60	120	
		15	40	40	80	
$t_{\text{su}}$	Minimum Setup Time, Parallel Data to Clock (Figure 4)	5.0	50	50	100	ns
		10	30	30	60	
		15	20	20	40	
$t_{\text{h}}$	Minimum Hold Time, Clock to Data (Figure 4)	5.0	50	50	100	ns
		10	15	15	30	
		15	10	10	20	
$t_{\text{w}}$	Minimum Pulse Width, AE, P/S, A/S (Figure 5)	5.0	350	350	700	ns
		10	140	140	280	
		15	80	80	160	
$t_{\text{w}}$	Minimum Pulse Width, Clock (Figure 2)	5.0	250	250	500	ns
		10	100	100	200	
		15	70	70	140	
$t_r$ , $t_f$	Minimum Input Rise or Fall Time, Clock (Figure 2)	5.0	15	15	30	ns
		10	15	15	30	
		15	15	15	30	

## TRUTH TABLE FOR REGISTER INPUT-LEVELS AND RESULTING REGISTER OPERATION

“A” Enable	P/S	A/B	A/S	Operation *
L	L	L	X	Serial Mode; Synch. Serial Data Input, “A” Parallel Data Outputs Disabled
L	L	H	X	Serial Mode, Synch. Serial Data Input, “B” Parallel Data Output
L	H	L	L	Parallel Mode; “B” Synch. Parallel Data Inputs, “A” Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; “B” Asynch. Parallel Data Inputs, “A” Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; “A” Parallel Data Inputs Disabled, “B” Parallel Data Outputs, Synch. Data Recirculation
L	H	H	H	Parallel Mode; “A” Parallel Data Inputs Disabled, “B” Parallel Data Outputs, Asynch. Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, “A” Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, “B” Parallel Data Output
H	H	L	L	Parallel Mode; “B” Synch. Parallel Data Input, “A” Parallel Data Output
H	H	L	H	Parallel Mode; “B” Asynch. Parallel Data Input, “A” Parallel Data Output
H	H	H	L	Parallel Mode; “A” Synch. Parallel Data Input, “B” Parallel Data Output
H	H	H	H	Parallel Mode; “A” Asynch. Parallel Data Input, “B” Parallel Data Output

\* Outputs change at positive transition of clock in the serial mode and when the A/S control input is “low” in the parallel mode. During transfer from parallel to serial operation A/S should remain low in order to prevent D<sub>S</sub> transfer into Flip Flops.

X = Don't Care

### PARALLEL OPERATION

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

### SERIAL OPERATION

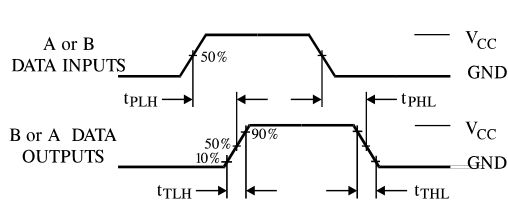
A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

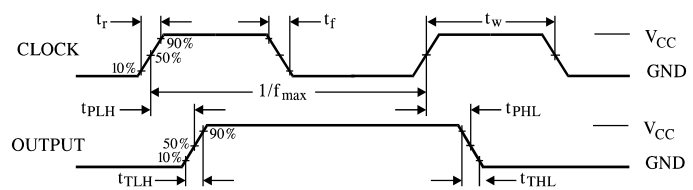
**FLIP-FLOP TRUTH TABLE**

Inputs			Output
$\overline{CL}_M$	$\overline{CL}_S$	D	Q
		L	L
		L	L
		L	INVALID CONDITION
		X	L
		H	H
		H	H
		H	INVALID CONDITION

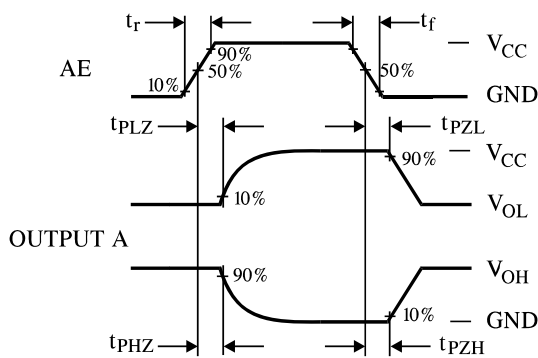
X = don't care



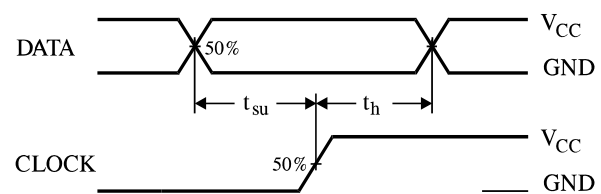
**Figure 1. Asynchronous operation**



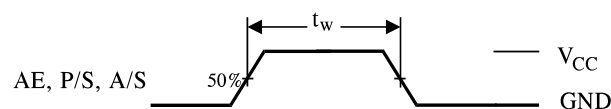
**Figure 2. Synchronous operation**



**Figure 3. Switching Waveforms**

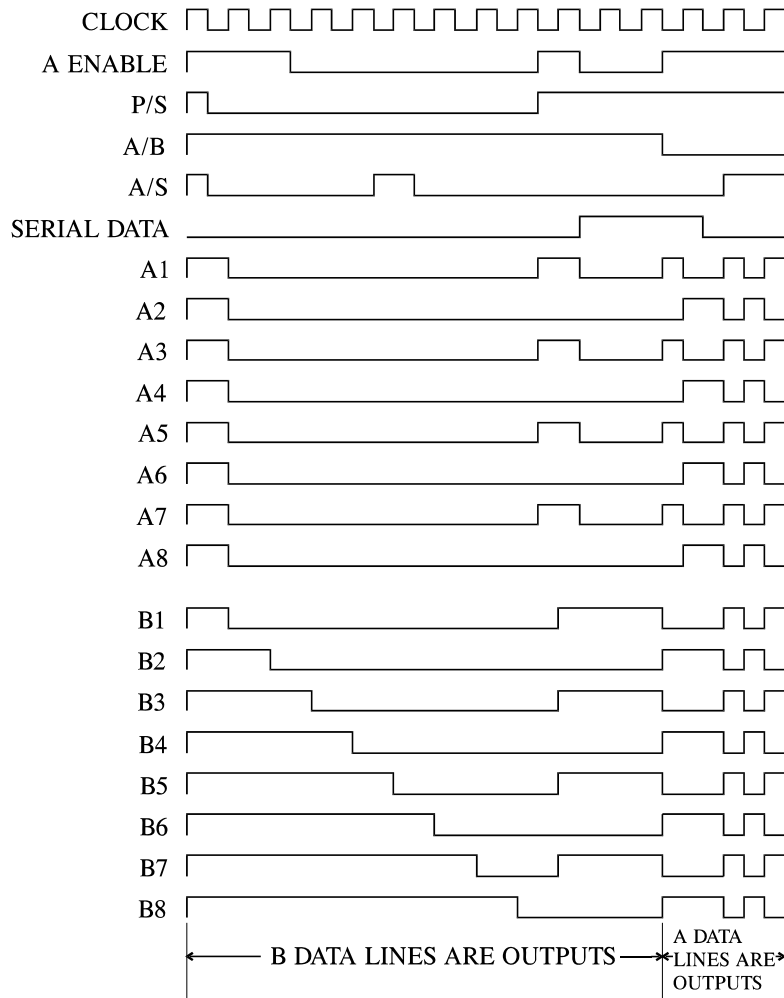


**Figure 4. Switching Waveforms**

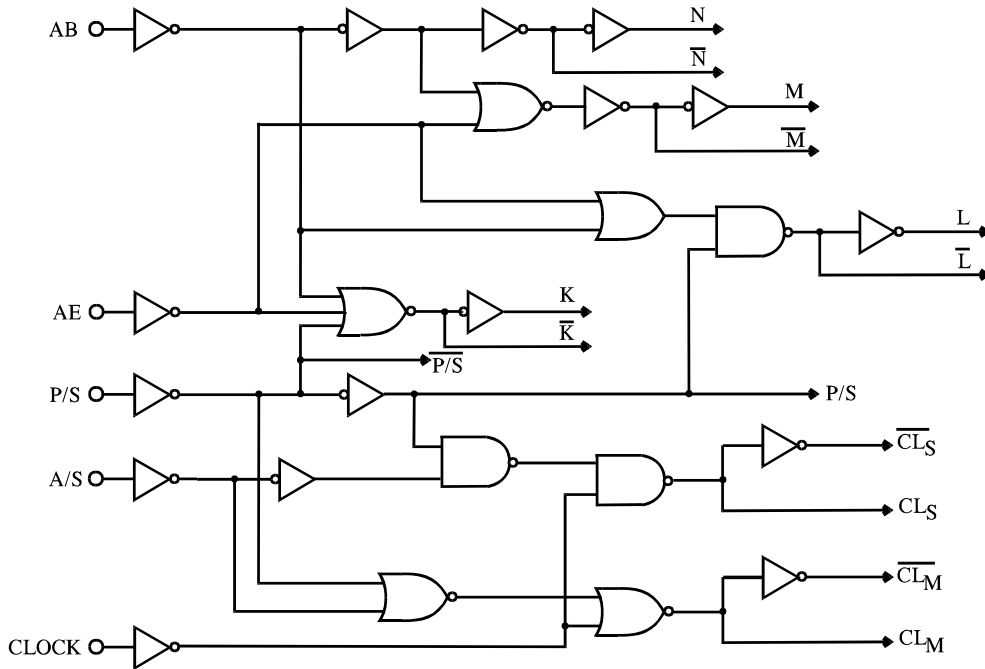


**Figure 5. Switching Waveforms**

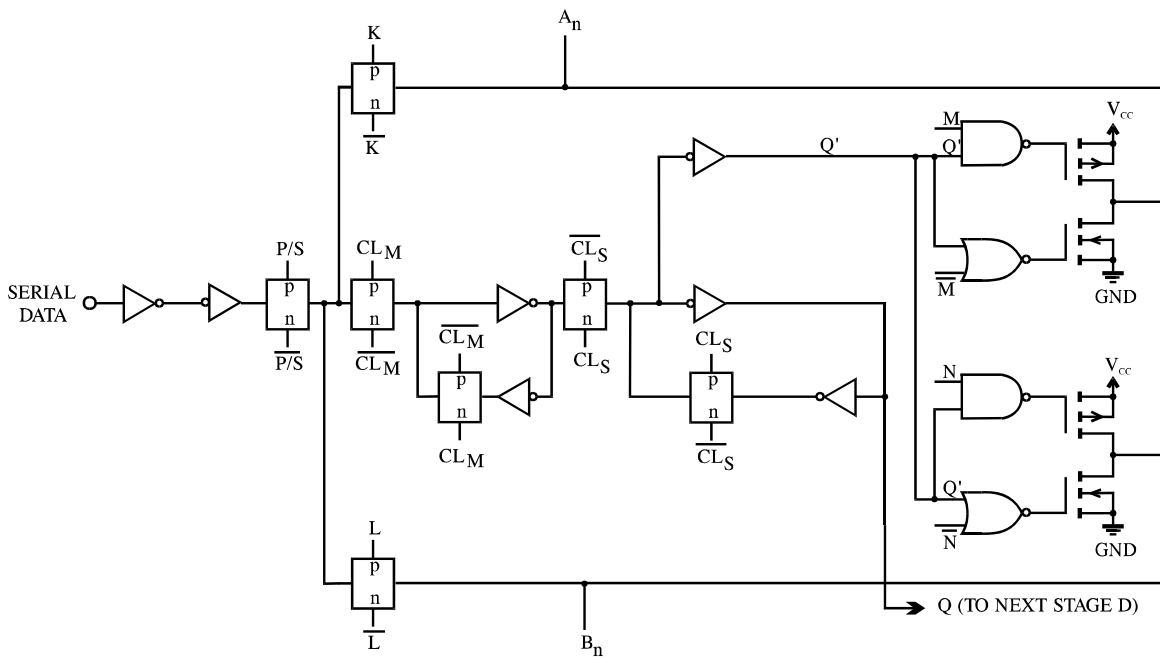
**TIMING DIAGRAM**



**EXPANDED LOGIC DIAGRAM**



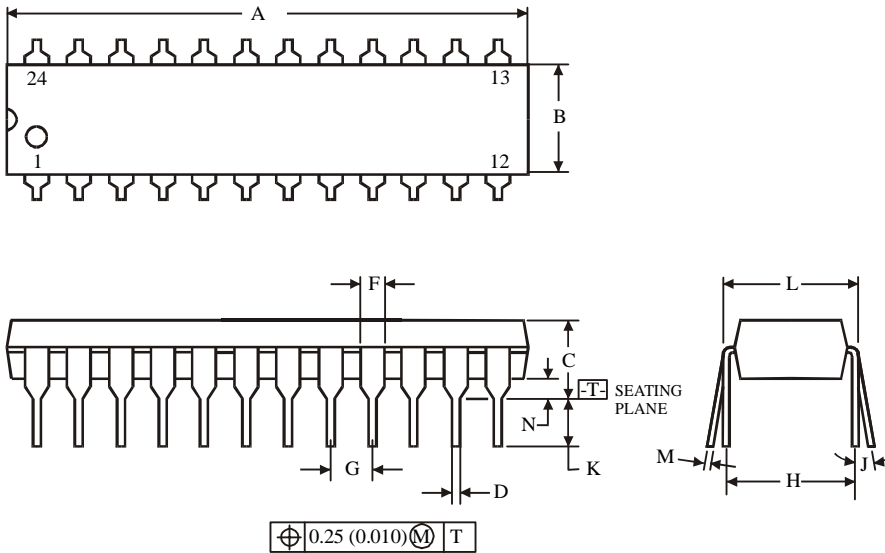
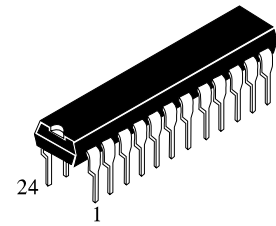
**Steering logic diagram**



**Register stage logic diagram (1/8 stages)**



**N SUFFIX PLASTIC  
(MS - 001AF)**

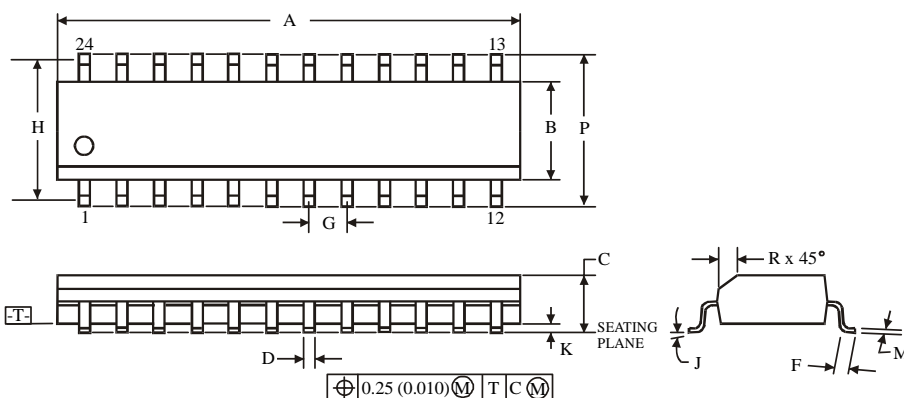
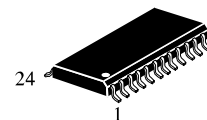


Symbol	Dimensions, mm	
	MIN	MAX
A	31.24	32.51
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	

**NOTES:**

1. Dimensions "A", "B" do not include mold flash or protrusions. Maximum mold flash or protrusions 0.25 mm (0.010) per side.

**DW SUFFIX SOIC  
(MS - 013AD)**



Symbol.	Dimensions, mm	
	MIN	MAX
A	15.20	15.60
B	7.40	7.60
C	2.35	2.65
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.10	0.30
M	0.23	0.32
P	10.0	10.65
R	0.25	0.75

**NOTES:**

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.