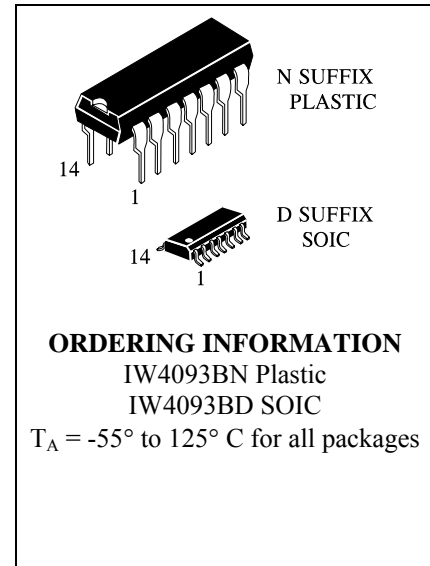


IW4093B

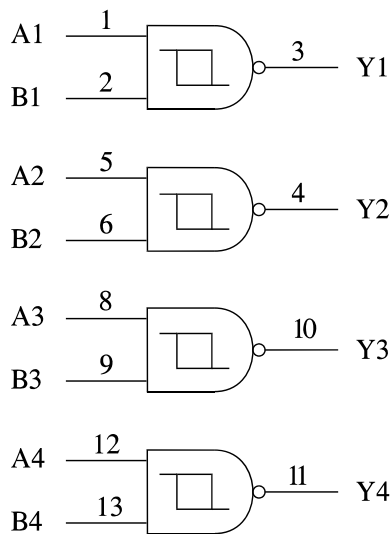
**Quad 2-Input NAND Schmitt Triggers
High-Voltage Silicon-Gate CMOS**

The IW4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_{T+}) and the negative voltage (V_{T-}) is defined as hysteresis voltage (V_H) (see Fig.1).

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 0.5 V min @ 5.0 V supply
 - 1.0 V min @ 10.0 V supply
 - 1.5 V min @ 15.0 V supply

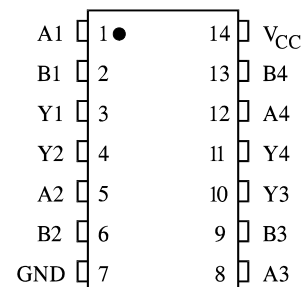


LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

L – LOW voltage level

H – HIGH voltage level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	500 500	mW
P _{tot}	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 12 mW/°C from 100° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{T+min}	Minimum Positive-Going Input Threshold Voltage	Input on terminals A or B; other inputs to V _{CC}	5.0	2.2	2.2	2.2	V
			10	4.6	4.6	4.6	
			15	6.8	6.8	6.8	
			5.0	2.6	2.6	2.6	
		Input on terminals A and B; other inputs to V _{CC}	10	5.6	5.6	5.6	
			15	6.3	6.3	6.3	
V _{T+max}	Maximum Positive-Going Input Threshold Voltage	Input on terminals A or B; other inputs to V _{CC}	5.0	3.6	3.6	3.6	V
			10	7.1	7.1	7.1	
		Input on terminals A and B; other inputs to V _{CC}	15	10.8	10.8	10.8	
			5.0	4	4	4	
		Input on terminals A and B; other inputs to V _{CC}	10	8.2	8.2	8.2	
			15	12.7	12.7	12.7	
V _{T-min}	Minimum Negative-Going Input Threshold Voltage	Input on terminals A or B; other inputs to V _{CC}	5.0	0.9	0.9	0.9	V
			10	2.5	2.5	2.5	
		Input on terminals A and B; other inputs to V _{CC}	15	4	4	4	
			5.0	1.4	1.4	1.4	
		Input on terminals A and B; other inputs to V _{CC}	10	3.4	3.4	3.4	
			15	4.8	4.8	4.8	
V _{T-max}	Maximum Negative-Going Input Threshold Voltage	Input on terminals A or B; other inputs to V _{CC}	5.0	2.8	2.8	2.8	V
			10	5.2	5.2	5.2	
		Input on terminals A and B; other inputs to V _{CC}	15	7.4	7.4	7.4	
			5.0	3.2	3.2	3.2	
		Input on terminals A and B; other inputs to V _{CC}	10	6.6	6.6	6.6	
			15	9.6	9.6	9.6	
V _{Hmin} Note	Minimum Hysteresis Voltage	Input on terminals A or B; other inputs to V _{CC}	5.0	0.3	0.3	0.3	V
			10	1.2	1.2	1.2	
		Input on terminals A and B; other inputs to V _{CC}	15	1.6	1.6	1.6	
			5.0	0.3	0.3	0.3	
		Input on terminals A and B; other inputs to V _{CC}	10	1.2	1.2	1.2	
			15	1.6	1.6	1.6	
V _{Hmax} Note	Maximum Hysteresis Voltage	Input on terminals A or B; other inputs to V _{CC}	5.0	1.6	1.6	1.6	V
			10	3.4	3.4	3.4	
		Input on terminals A and B; other inputs to V _{CC}	15	5	5	5	
			5.0	1.6	1.6	1.6	
		Input on terminals A and B; other inputs to V _{CC}	10	3.4	3.4	3.4	
			15	5	5	5	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) - continued

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	1	1	30	μA
			10	2	2	60	
			15	4	4	120	
			20	20	20	600	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2.0	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	

Note. V_{Hmin}>(V_{T+.min})-(V_{T-.max}); V_{Hmax}=(V_{T+.max})+(V_{T-.min}).

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=200kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			≥-55°C	25°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figure 2)	5.0	380	380	760	ns
		10	180	180	360	
		15	130	130	260	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figure 2)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
C _{IN}	Maximum Input Capacitance	-		7.5		pF

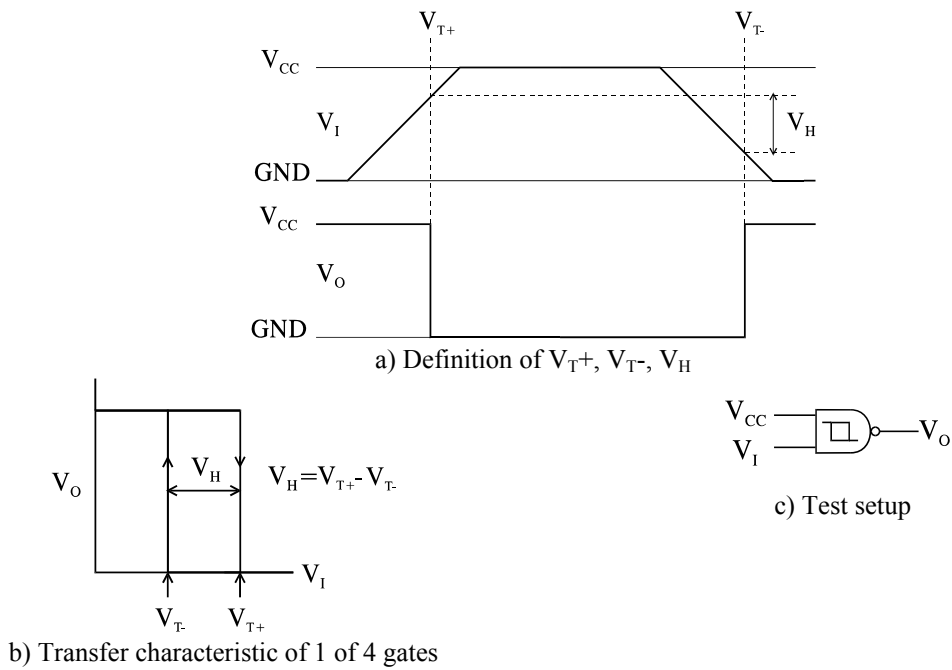


Figure 1. Hysteresis definition, characteristic, and test setup

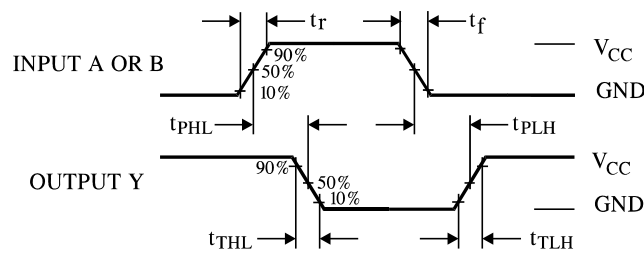
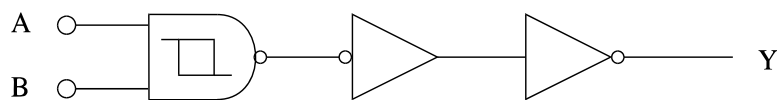
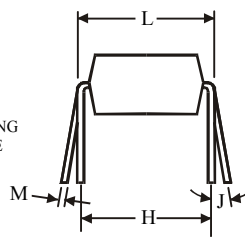
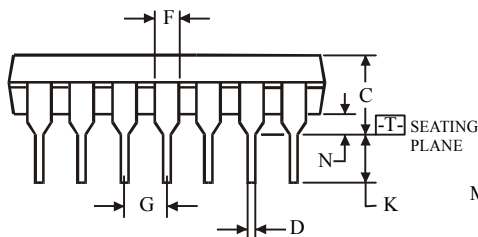
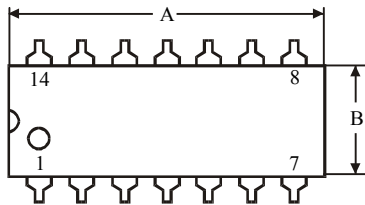
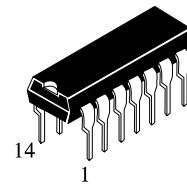


Figure 2. Switching Waveforms

**EXPANDED LOGIC DIAGRAM
(1/4 of the Device)**



**N SUFFIX PLASTIC DIP
(MS - 001AA)**



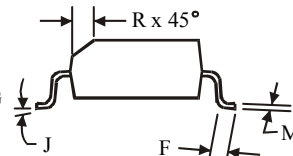
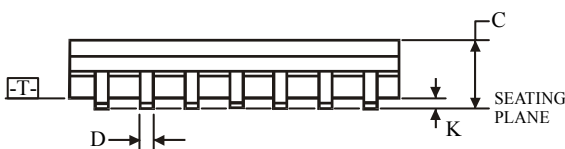
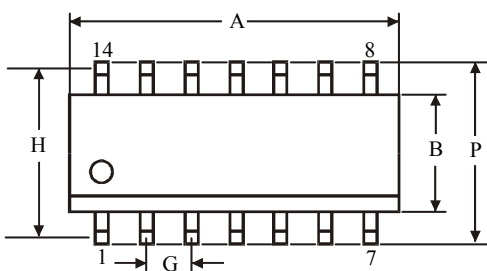
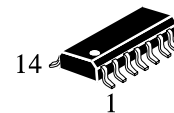
$\oplus 0.25 (0.010) \text{ (M) T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Dimension, mm		
Symbol	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**D SUFFIX SOIC
(MS - 012AB)**



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Dimension, mm		
Symbol	MIN	MAX
A	8.55	8.75
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.27	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5